Rochester Electronics

Datasheet

PART NUMBER

54AC251^QFA

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All re-creations are done with the approval of the Original Component Manufacturer. (OCM)

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
    - Class Q Military
    - Class V Space Level

Qualified Suppliers List of Distributors (QSLD)

- Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OCM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

54AC251 • 54ACT251 8-Input Multiplexer with TRI-STATE Output

Check for Samples: 54AC251, 54ACT251

FEATURES

- **I_{CC} Reduced by 50%**
- **Multifunctional Capability**
- **On-Chip Select Logic Decoding**
- **Inverting and Noninverting TRI-STATE Outputs**
- **Outputs Source/Sink 24 mA**
- **'ACT251 has TTL-Compatible Inputs**
- **Standard Military Drawing (SMD)**
  - **'AC251: 5962-87692**
  - **'ACT251: 5962-89599**

DESCRIPTION

The 'AC/'ACT251 is a high-speed 8-input digital multiplexer. It provides, in one package, the ability to select one bit of data from up to eight sources. It can be used as universal function generator to generate any logic function of four variables. Both true and complementary outputs are provided.

Logic Symbols

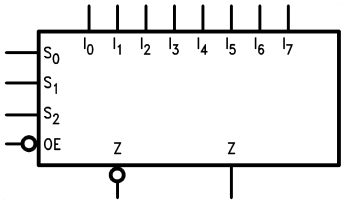

Figure 1.

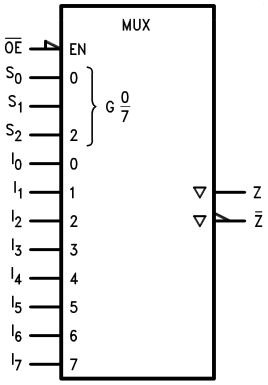

Figure 2. IEEE/IEC

PIN DESCRIPTION

Pin Names	Description
S_0–S_2	Select Inputs
$\overline{OE}$	TRI-STATE Output Enable Input
I_0–I_7	Multiplexer Inputs
Z	TRI-STATE Multiplexer Output
$\overline{Z}$	Complementary TRI-STATE Multiplexer
	Output

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Connection Diagram

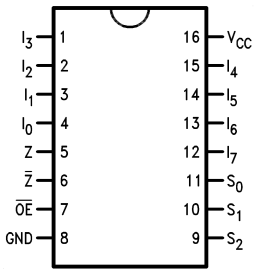

Figure 3. 16-Pin CERDIP or CLGA
See NAD0016A Package

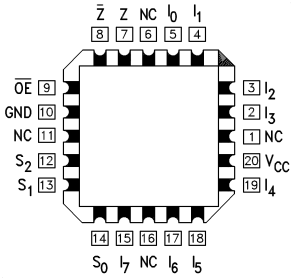

Figure 4. 20-Pin LCCC
See NAJ0020A Package

FUNCTIONAL DESCRIPTION

This device is a logical implementation of a single-pole, 8-position switch with the switch position controlled by the state of three Select inputs, S_0, S_1, S_2. Both true and complementary outputs are provided. The Output Enable input ($\overline{OE}$) is active LOW. When it is activated, the logic function provided at the output is:

$$\mathbf{Z = \overline{OE} \bullet} (I_0 \bullet \overline{S}_0 \bullet \overline{S}_1 \bullet \overline{S}_2 + I_1 \bullet S_0 \bullet \overline{S}_1 \bullet \overline{S}_2 +$$
$$I_2 \bullet \overline{S}_0 \bullet S_1 \bullet \overline{S}_2 + I_3 \bullet S_0 \bullet S_1 \bullet \overline{S}_2 +$$
$$I_4 \bullet \overline{S}_0 \bullet \overline{S}_1 \bullet S_2 + I_5 \bullet S_0 \bullet \overline{S}_1 \bullet S_2 +$$
$$I_6 \bullet \overline{S}_0 \bullet S_1 \bullet S_2 + I_7 \bullet S_0 \bullet S_1 \bullet S_2)$$

When the Output Enable is HIGH, both outputs are in the high impedance (High Z) state. This feature allows multiplexer expansion by tying the outputs of up to 128 devices together. When the outputs of the TRI-STATE devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. The Output Enable signals should be designed to ensure there is no overlap in the active-LOW portion of the enable voltages.

TRUTH TABLE (1)

Inputs				Outputs	
$\overline{OE}$	S_2	S_1	S_0	$\overline{Z}$	Z
H	X	X	X	Z	Z
L	L	L	L	$\overline{I}_0$	I_0
L	L	L	H	$\overline{I}_1$	I_1
L	L	H	L	$\overline{I}_2$	I_2
L	L	H	H	$\overline{I}_3$	I_3
L	H	L	L	$\overline{I}_4$	I_4
L	H	L	H	$\overline{I}_5$	I_5
L	H	H	L	$\overline{I}_6$	I_6
L	H	H	H	$\overline{I}_7$	I_7

(1) H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

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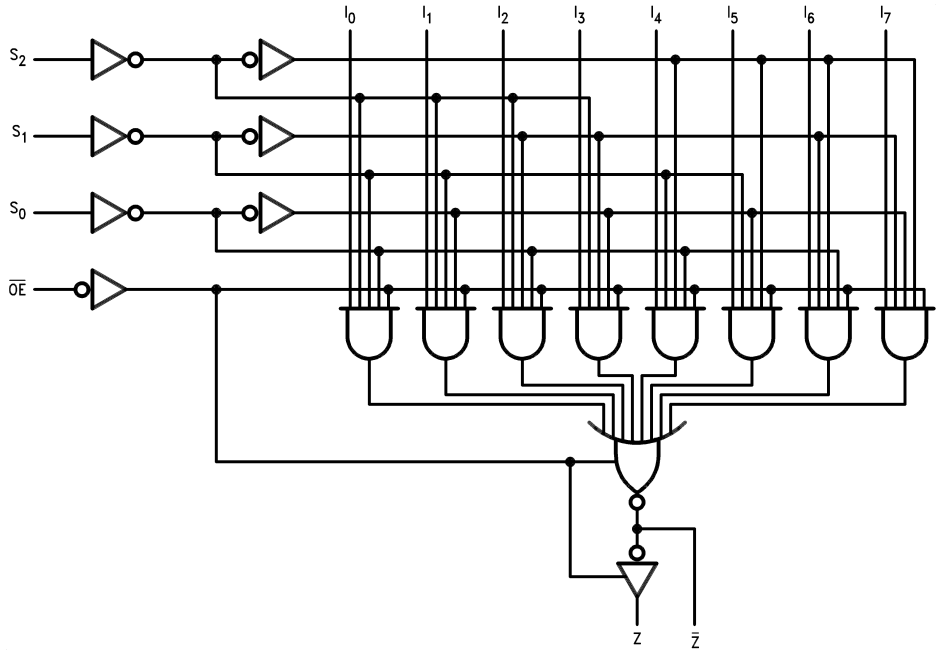
Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS (1)(2)

Supply Voltage (V_{CC})		−0.5V to +7.0V
DC Input Diode Current (I_{IK})	V_I = −0.5V	−20 mA
	V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)		−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	V_O = −0.5V	−20 mA
	V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)		−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)		±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})		±50 mA
Storage Temperature (T_{STG})		−65°C to +150°C
Junction Temperature (T_J)	CDIP	175°C

(1) Absolute Maximum Ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Texas Instruments does not recommend operation of FACT® circuits outside databook specifications.

(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage (V_{CC})	'AC	2.0V to 6.0V
	'ACT	4.5V to 5.5V
Input Voltage (V_I)		0V to V_{CC}
Output Voltage (V_O)		0V to V_{CC}
Operating Temperature (T_A)	54AC/ACT	−55°C to +125°C
Minimum Input Edge Rate (ΔV/Δt) 'AC Devices	V_{IN} from 30% to 70% of V_{CC}	
	V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate (ΔV/Δt) 'ACT Devices	V_{IN} from 0.8V to 2.0V	
	V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC CHARACTERISTICS FOR 'AC FAMILY DEVICES

Symbol	Parameter	V_{CC} (V)	54AC T_A = −55°C to +125°C Ensured Limits	Units	Conditions
V_{IH}	Minimum High Level Input Voltage	3.0	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	3.15		
		5.5	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	1.35		
		5.5	1.65		

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DC CHARACTERISTICS FOR 'AC FAMILY DEVICES (continued)

Symbol	Parameter	V_{CC} (V)	54AC T_A = −55°C to +125°C Ensured Limits	Units	Conditions
V_{OH}	Minimum High Level Output Voltage	3.0 4.5 5.5	2.9 4.4 5.4	V	I_{OUT} = −50 µA
		3.0 4.5 5.5	2.4 3.7 4.7	V	V_{IN} = V_{IL} or V_{IH} (1) I_{OH} = −12 mA I_{OH} = −24 mA I_{OH} = −24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0 4.5 5.5	0.1 0.1 0.1	V	I_{OUT} = 50 µA
		3.0 4.5 5.5	0.50 0.50 0.50	V	V_{IN} = V_{IL} or V_{IH} (1) I_{OL} = 12 mA I_{OL} = 24 mA I_{OL} = 24 mA
I_{IN}	Maximum Input Leakage Current	5.5	±1.0	µA	V_I = V_{CC}, GND
I_{OZ}	Maximum TRI-STATE Current	5.5	±5.0	µA	V_I (OE) = V_{IL}, V_{IH} V_I = V_{CC}, V_{GND} V_O = V_{CC}, GND
I_{OLD}	Minimum Dynamic Output Current (2)	5.5	50	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5	−50	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5	80.0	µA	V_{IN} = V_{CC} or GND

(1) All outputs loaded; thresholds on input associated with output under test.
(2) Maximum test duration 2.0 ms, one output loaded at a time.

DC CHARACTERISTICS FOR 'ACT FAMILY DEVICES

Symbol	Parameter	V_{CC} (V)	54ACT T_A = −55°C to +125°C Ensured Limits	Units	Conditions
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.4 5.4	V	I_{OUT} = −50 µA
		4.5 5.5	3.70 4.70	V	V_{IN} = V_{IL} or V_{IH} (1) I_{OH} = −24 mA I_{OH} = −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.1 0.1	V	I_{OUT} = 50 µA
		4.5 5.5	0.50 0.50	V	V_{IN} = V_{IL} or V_{IH} (1) I_{OL} = 24 mA I_{OL} = 24 mA

(1) All outputs loaded; thresholds on input associated with output under test.

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DC CHARACTERISTICS FOR 'ACT FAMILY DEVICES (continued)

Symbol	Parameter	V_{CC} (V)	54ACT T_A = −55°C to +125° Ensured Limits	Units	Conditions
I_{IN}	Maximum Input Leakage Current	5.5	±1.0	µA	$V_I = V_{CC}$, GND
I_{OZ}	Maximum TRI-STATE Current	5.5	±5.0	µA	$V_I = V_{IL}, V_{IH}$ $V_O = V_{CC}$, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	1.6	mA	$V_I = V_{CC}$ − 2.1V
I_{OLD}	Minimum Dynamic Output Current (2)	5.5	50	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5	−50	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5	80.0	µA	$V_{IN} = V_{CC}$ or GND

(2) Maximum test duration 2.0 ms, one output loaded at a time.

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V_{CC} (V) (1)	54AC T_A = −55°C to +125°C C_L = 50 pF		Units
			Min	Max	
t_{PLH}	Propagation Delay S_n to Z or $\overline{Z}$	3.3	1.0	21.0	ns
		5.0	1.0	15.5	
t_{PHL}	Propagation Delay S_n to Z or $\overline{Z}$	3.3	1.0	21.0	ns
		5.0	1.0	15.5	
t_{PLH}	Propagation Delay I_n to Z or $\overline{Z}$	3.3	1.0	17.0	ns
		5.0	1.0	12.0	
t_{PHL}	Propagation Delay I_n to Z or $\overline{Z}$	3.3	1.0	16.5	ns
		5.0	1.0	12.0	
t_{PZH}	Output Enable Time $\overline{OE}$ to Z or $\overline{Z}$	3.3	1.0	13.0	ns
		5.0	1.0	10.0	
t_{PZL}	Output Enable Time $\overline{OE}$ to Z or $\overline{Z}$	3.3	1.0	13.0	ns
		5.0	1.0	10.0	
t_{PHZ}	Output Disable Time $\overline{OE}$ to Z or $\overline{Z}$	3.3	3.5	14.0	ns
		5.0	2.5	11.0	
t_{PLZ}	Output Disable Time $\overline{OE}$ to Z or $\overline{Z}$	3.3	4.0	13.0	ns
		5.0	3.0	10.0	

(1) Voltage Range 3.3 is 3.3V ±0.3V Voltage Range 5.0 is 5.0V ±0.5V.

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V_{CC} (V) (1)	54ACT T_A = −55°C to +125°C C_L = 50 pF		Units
			Min	Max	
t_{PLH}	Propagation Delay S_n to Z or $\overline{Z}$	5.0	1.0	18.0	ns
t_{PHL}	Propagation Delay S_n to Z or $\overline{Z}$	5.0	1.0	18.0	ns
t_{PLH}	Propagation Delay I_n to Z or $\overline{Z}$	5.0	1.0	13.5	ns
t_{PHL}	Propagation Delay I_n to Z or $\overline{Z}$	5.0	1.0	13.5	ns
t_{PZH}	Output Enable Time $\overline{OE}$ to Z or $\overline{Z}$	5.0	1.0	10.0	ns
t_{PZL}	Output Enable Time $\overline{OE}$ to Z or $\overline{Z}$	5.0	1.0	9.5	ns

(1) Voltage Range 5.0 is 5.0V ±0.5V.

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AC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	V_{CC} (V) (1)	54ACT T_A = −55°C to +125°C C_L = 50 pF		Units
			Min	Max	
t_{PHZ}	Output Disable Time $\overline{OE}$ to Z or $\overline{Z}$	5.0	1.0	12.5	ns
t_{PLZ}	Output Disable Time $\overline{OE}$ to Z or $\overline{Z}$	5.0	1.0	8.5	ns

CAPACITANCE

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = OPEN
C_{PD}	Power Dissipation Capacitance	70.0	pF	V_{CC} = 5.0V

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REVISION HISTORY

Changes from Revision A (April 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	7

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