

## Description

The 9FGL02x1/04x1/06x1/08x1 devices comprise a family of 3.3V PCIe Gen1–5 clock generators. There are 2, 4, 6 and 8 outputs versions available and each differential output has a dedicated OE# pin supporting PCIe CLKREQ# functionality.

## PCIe Clocking Architectures

- Common Clocked (CC)
- Independent Reference (IR) with and without spread spectrum (SRIS, SRNS)

## Typical Applications

- Servers/High-Performance Computing
- nVME Storage
- Networking
- Accelerators
- Industrial Control

## Output Features

- 2, 4, 6, or 8 100MHz PCIe output pairs
- One 3.3V LVCMOS REF output with Wake-On-LAN (WOL) support
- See [AN-891](#) for easy AC-coupling to other logic families

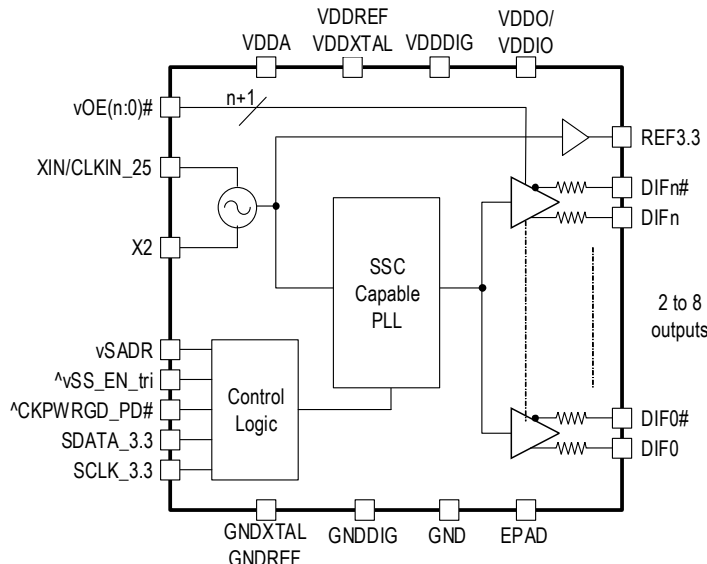
## Key Specifications

- 90fs RMS typical jitter (PCIe Gen5 CC)
- < 50ps cycle-to-cycle jitter on differential outputs
- < 50ps output-to-output skew on differential outputs
- ±0ppm synthesis error on differential outputs

## Features

- Integrated terminations for 100Ω and 85Ω systems save 4 resistors per output
- 112–206 mW typical power consumption (at 3.3V)
- V<sub>DDIO</sub> rail allows 35% power savings at optional 1.05V (9FGL06 and 9FGL08 only)
- Devices contain default configuration; SMBus not required
- SMBus-selectable features allows optimization to customer requirements:
  - Input polarity and pull-up/pull-downs
  - Output slew rate and amplitude
  - Output impedance (33Ω, 85Ω or 100Ω) for each output
- Contact factory for customized default configurations
- 25MHz input frequency
- OE# pins support PCIe CLKREQ# function
- Pin-selectable SRnS 0%, CC 0% and CC/SRIS -0.5% spread
- SMBus-selectable CC/SRIS -0.25% spread
- Clean switching between the CC/SRIS spread settings
- DIF outputs blocked until PLL is locked; clean system start-up
- Two selectable SMBus addresses
- Space saving packages:
  - 4 × 4 mm 24-VFQFPN (9FGL02x1)
  - 5 × 5 mm 32-VFQFPN (9FGL04x1)
  - 5 × 5 mm 40-VFQFPN (9FGL06x1)
  - 6 × 6 mm 48-VFQFPN (9FGL08x1)

## Block Diagram



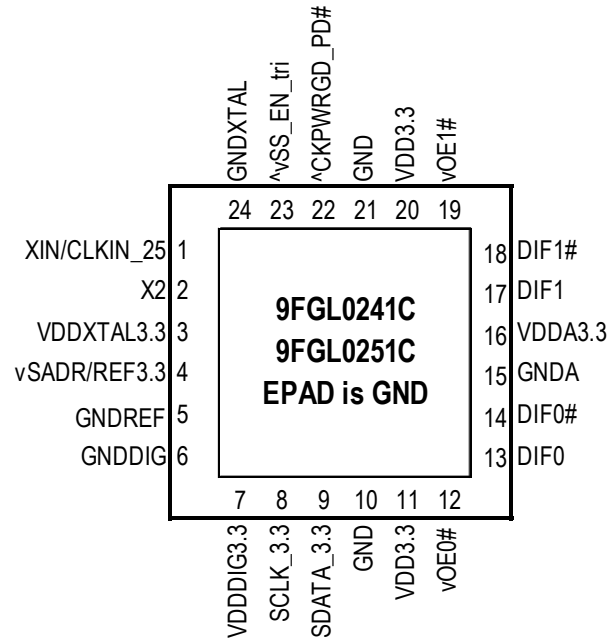
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## Pin Assignments

### 9FGL02x1 Pin Assignment

Figure 1. Pin Assignments for 4 × 4 mm 24-VFQFPN Package – Top View



#### 24-VFQFPN, 4 x 4 mm, 0.5mm pitch

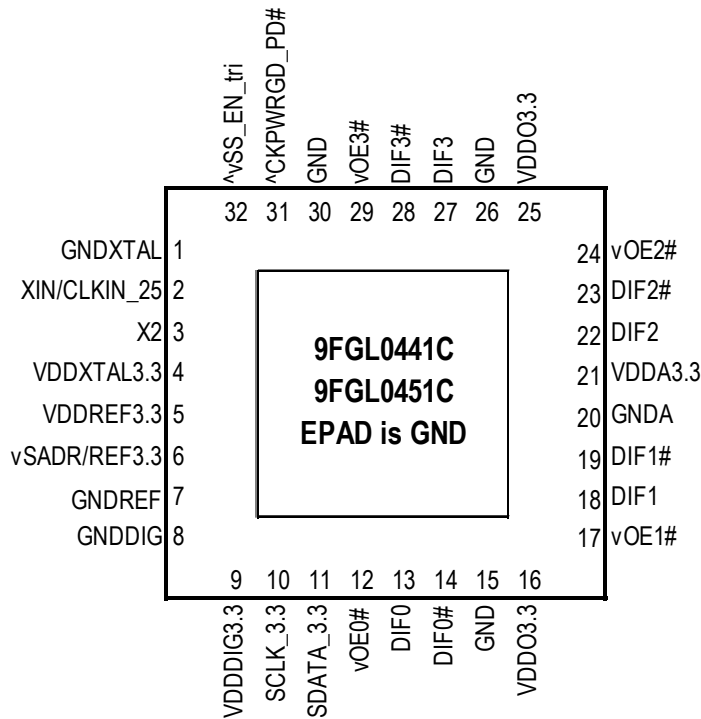
^ prefix indicates internal 120kOhm pull-up resistor

v prefix indicates internal 120kOhm pull-down resistor

^v prefix indicates internal 120kOhm pull-up and pull-down resistors

## 9FGL04x1 Pin Assignment

Figure 2. Pin Assignments for 5 × 5 mm 32-VFQFPN Package – Top View



### 32-VFQFPN, 5 x 5 mm, 0.5mm pitch

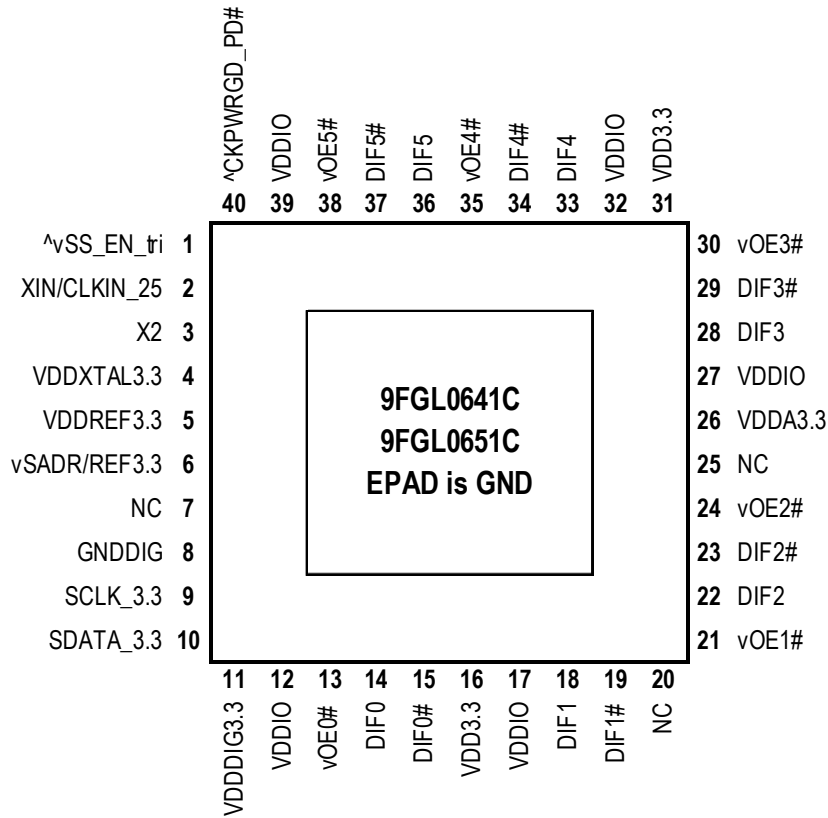
^ prefix indicates internal 120kOhm pull-up resistor

v prefix indicates internal 120kOhm pull-down resistor

^v prefix indicates internal 120kOhm pull-up and pull-down resistors

### 9FGL06x1 Pin Assignment

Figure 3. Pin Assignments for 5 × 5 mm 40-VFQFPN Package – Top View



**40-VFQFPN, 5 x 5 mm, 0.4mm pitch**

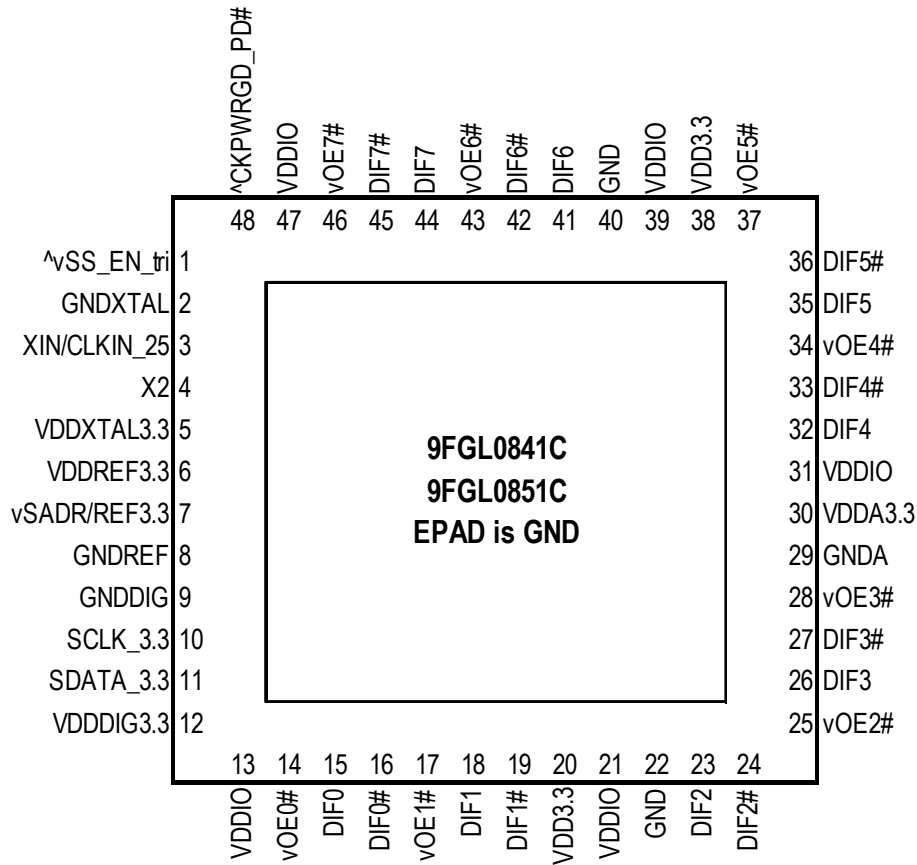
^ prefix indicates internal 120kOhm pull-up resistor

v prefix indicates internal 120kOhm pull-down resistor

^v prefix indicates internal 120kOhm pull-up and pull-down resistors

## 9FGL08x1 Pin Assignment

Figure 4. Pin Assignments for 6 × 6 mm 48-VFQFPN Package – Top View



### 48-VFQFPN, 6 x 6 mm, 0.4mm pitch

^ prefix indicates internal pull-up resistor

v prefix indicates internal pull-down resistor

^v prefix indicates internal pull-up and pull-down resistors

## Pin Descriptions

Table 1. Pin Descriptions

Name	Type	Description	9FGL08x1 Pin No.	9FGL06x1 Pin No.	9FGL04x1 Pin No.	9FGL02x1 Pin No.
^CKPWRGD_PD#	Input	Input notifies device to sample latched inputs and start up on first high assertion. Low enters Power Down Mode, subsequent high assertions exit Power Down Mode. This pin has internal pull-up resistor.	48	40	31	22
^vSS_EN_tri	Latched In	Latched select input to select spread spectrum amount at initial power up. See <a href="#">Spread Selection</a> table.	1	1	32	23
DIF0	Output	Differential true clock output.	15	14	13	13
DIF0#	Output	Differential complementary clock output.	16	15	14	14
DIF1	Output	Differential true clock output.	18	18	18	17

**Table 1. Pin Descriptions (Cont.)**

Name	Type	Description	9FGL08x1 Pin No.	9FGL06x1 Pin No.	9FGL04x1 Pin No.	9FGL02x1 Pin No.
DIF1#	Output	Differential complementary clock output.	19	19	19	18
DIF2	Output	Differential true clock output.	23	22	22	-
DIF2#	Output	Differential complementary clock output.	24	23	23	-
DIF3	Output	Differential true clock output.	26	28	27	-
DIF3#	Output	Differential complementary clock output.	27	29	28	-
DIF4	Output	Differential true clock output.	32	33	-	-
DIF4#	Output	Differential complementary clock output.	33	34	-	-
DIF5	Output	Differential true clock output.	35	36	-	-
DIF5#	Output	Differential complementary clock output.	36	37	-	-
DIF6	Output	Differential true clock output.	41	-	-	-
DIF6#	Output	Differential complementary clock output.	42	-	-	-
DIF7	Output	Differential true clock output.	44	-	-	-
DIF7#	Output	Differential complementary clock output.	45	-	-	-
EPAD	GND	Connect to ground.	49	41	33	25
GND	GND	Ground pin.	22	EPAD	15	10
GND	GND	Ground pin.	40	EPAD	26, 30	21
GND A	GND	Ground pin for the PLL core.	29	EPAD	20	15
GNDDIG	GND	Ground pin for digital circuitry.	9	8	8	6
GNDREF	GND	Ground pin for the REF outputs.	8	-	7	5
GNDXTAL	GND	GND for XTAL.	2	EPAD	1	24
NC	—	No connect.	-	7, 25	-	-
SCLK_3.3	Input	Clock pin of SMBus circuitry, 3.3V tolerant.	10	9	10	8
SDATA_3.3	I/O	Data pin for SMBus circuitry, 3.3V tolerant.	11	10	11	9
VDD3.3	Power	Power supply, nominally 3.3V.	20	16	16	11
VDD3.3	Power	Power supply, nominally 3.3V.	38	31	25	20
VDDA3.3	Power	3.3V power for the PLL core.	30	26	21	16
VDDDIG3.3	Power	3.3V digital power (dirty power).	12	11	9	7
VDDIO	Power	Power supply for differential outputs.	13	12	-	-
VDDIO	Power	Power supply for differential outputs.	21	17	-	-
VDDIO	Power	Power supply for differential outputs.	31	27	-	-
VDDIO	Power	Power supply for differential outputs.	39	32	-	-
VDDIO	Power	Power supply for differential outputs.	47	39	-	-
VDDREF3.3	Power	Power supply for REF output, nominally 3.3V.	6	5	5	-
VDDXTAL3.3	Power	Power supply for XTAL, nominally 3.3V.	5	4	4	3

**Table 1. Pin Descriptions (Cont.)**

Name	Type	Description	9FGL08x1 Pin No.	9FGL06x1 Pin No.	9FGL04x1 Pin No.	9FGL02x1 Pin No.
vOE0#	Input	Active low input for enabling output 0. This pin has an internal pull-down. 1 = disable output, 0 = enable output.	14	13	12	12
vOE1#	Input	Active low input for enabling output 1. This pin has an internal pull-down. 1 = disable output, 0 = enable output.	17	21	17	19
vOE2#	Input	Active low input for enabling output 2. This pin has an internal pull-down. 1 = disable output, 0 = enable output.	25	24	24	-
vOE3#	Input	Active low input for enabling output 3. This pin has an internal pull-down. 1 = disable output, 0 = enable output.	28	30	29	-
vOE4#	Input	Active low input for enabling output 4. This pin has an internal pull-down. 1 = disable output, 0 = enable output.	34	35	-	-
vOE5#	Input	Active low input for enabling output 5. This pin has an internal pull-down. 1 = disable output, 0 = enable output.	37	38	-	-
vOE6#	Input	Active low input for enabling output 6. This pin has an internal pull-down. 1 = disable output, 0 = enable output.	43	-	-	-
vOE7#	Input	Active low input for enabling output 7. This pin has an internal pull-down. 1 = disable output, 0 = enable output.	46	-	-	-
vSADR/REF3.3	Latched I/O	Latch to select SMBus Address/3.3V LVCMOS copy of X1/REFIN pin.	7	6	6	4
X2	Output	Crystal output.	4	3	3	2
XIN/CLKIN_25	Input	Crystal input or Reference Clock input, nominally 25MHz.	3	2	2	1

**Table 2. Spread Selection**

$\wedge$ vSS_EN_tri Pin	B1[4:3]	Spread%	Note
0	00	0	PCIe SRNS mode.
—	01	-0.25	PCIe Common Clock or SRIS mode.
M (VDD/2)	10	0	PCIe Common Clock or SRIS mode.
1	11	-0.50	PCIe Common Clock or SRIS mode.

If SRnS mode is desired, power up with  $\wedge$ vSS\_EN\_tri = '0'. Do not attempt to switch to the other modes via SMBus control in Byte 1 or a system reset will be required. If Common Clock (CC) or SRIS mode is desired, power up with  $\wedge$ vSS\_EN\_tri at either 'M' or '1'. The desired spread spectrum amount can then be selected via Byte 1 without a requiring a system reset. Once 'M' or '1' is latched at power up, do not attempt to enter SRnS mode or a system reset will be required.

## Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the 9FGL02x1/04x1/06x1/08x1 at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

**Table 3. Absolute Maximum Ratings**

Parameter	Symbol	Conditions	Minimum	Maximum	Unit	Notes
Supply Voltage	$V_{DDx}$		-0.5	4.6	V	1,2
Input Voltage	$V_{IN}$		-0.5	$V_{DD} + 0.5$	V	1,3
Input High Voltage, SMBus	$V_{IHSMB}$	SMBus clock and data pins.	-	$V_{DD} + 0.5$	V	1,3
Storage Temperature	$T_s$		-65	150	°C	1
Junction Temperature	$T_j$		-	125	°C	1
Input ESD Protection	ESD prot	Human Body Model.	2500	-	V	1

<sup>1</sup> Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup> Operation under these conditions is neither implied nor guaranteed.

<sup>3</sup> Not to exceed 4.6V.

## Thermal Characteristics

**Table 4. Thermal Characteristics**

Parameter	Symbol	Conditions	Package	Typical Values	Unit	Notes
9FGL02 Thermal Resistance	$\theta_{JC}$	Junction to case.	NLG24	62	°C/W	1
	$\theta_{Jb}$	Junction to base.		5.4	°C/W	1
	$\theta_{JA0}$	Junction to air, still air.		50	°C/W	1
	$\theta_{JA1}$	Junction to air, 1 m/s air flow.		43	°C/W	1
	$\theta_{JA3}$	Junction to air, 3 m/s air flow.		39	°C/W	1
	$\theta_{JA5}$	Junction to air, 5 m/s air flow.		38	°C/W	1
9FGL04 Thermal Resistance	$\theta_{JC}$	Junction to case.	NLG32	42	°C/W	1
	$\theta_{Jb}$	Junction to base.		2.4	°C/W	1
	$\theta_{JA0}$	Junction to air, still air.		39	°C/W	1
	$\theta_{JA1}$	Junction to air, 1 m/s air flow.		33	°C/W	1
	$\theta_{JA3}$	Junction to air, 3 m/s air flow.		28	°C/W	1
	$\theta_{JA5}$	Junction to air, 5 m/s air flow.		27	°C/W	1
9FGL06 Thermal Resistance	$\theta_{JC}$	Junction to case.	NDG40	42	°C/W	1
	$\theta_{Jb}$	Junction to base.		2.4	°C/W	1
	$\theta_{JA0}$	Junction to air, still air.		39	°C/W	1
	$\theta_{JA1}$	Junction to air, 1 m/s air flow.		33	°C/W	1
	$\theta_{JA3}$	Junction to air, 3 m/s air flow.		28	°C/W	1
	$\theta_{JA5}$	Junction to air, 5 m/s air flow.		27	°C/W	1

**Table 4. Thermal Characteristics (Cont.)**

Parameter	Symbol	Conditions	Package	Typical Values	Unit	Notes
9FGL08 Thermal Resistance	$\theta_{JC}$	Junction to case.	NDG48	33	°C/W	1
	$\theta_{Jb}$	Junction to base.		2.1	°C/W	1
	$\theta_{JA0}$	Junction to air, still air.		37	°C/W	1
	$\theta_{JA1}$	Junction to air, 1 m/s air flow.		30	°C/W	1
	$\theta_{JA3}$	Junction to air, 3 m/s air flow.		27	°C/W	1
	$\theta_{JA5}$	Junction to air, 5 m/s air flow.		26	°C/W	1

<sup>1</sup> EPAD soldered to board.

## Electrical Characteristics

$T_A = T_{AMB}$ . Supply voltages per normal operation conditions; see [Test Loads](#) for loading conditions.

**Table 5. SMBus Parameters**

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit	Notes
SMBus Input Low Voltage	$V_{ILSMB}$	$V_{DDSMB} = 3.3V$ .	-	-	0.8	V	-
SMBus Input High Voltage	$V_{IHSMB}$	$V_{DDSMB} = 3.3V$ .	2.1	-	3.6	V	-
SMBus Output Low Voltage	$V_{OLSMB}$	At $I_{PULLUP}$ .	-	-	0.4	V	-
SMBus Sink Current	$I_{PULLUP}$	At $V_{OL}$ .	4	-	-	mA	-
Nominal Bus Voltage	$V_{DDSMB}$		2.7	-	3.6	V	-
SCLK/SDATA Rise Time	$t_{RSMB}$	(Max. $V_{IL} - 0.15V$ ) to (Min. $V_{IH} + 0.15V$ ).	-	-	1000	ns	1
SCLK/SDATA Fall Time	$t_{FSMB}$	(Min. $V_{IH} + 0.15V$ ) to (Max. $V_{IL} - 0.15V$ ).	-	-	300	ns	1
SMBus Operating Frequency	$f_{SMB}$	SMBus operating frequency.	-	-	500	kHz	2

<sup>1</sup> Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup> The device must be powered up for the SMBus to function.

**Table 6. Input/Supply/Common Parameters – Normal Operating Conditions**

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit	Notes
Supply Voltage	$V_{DDxxx}$	Supply voltage for core, analog and single-ended LVCMOS outputs.	3.135	3.3	3.465	V	-
IO Supply Voltage	$V_{DDIO}$	Supply voltage for differential low power outputs.	0.9975	1.05–3.3	3.465	V	-
Ambient Operating Temperature	$T_{AMB}$	Industrial range.	-40	25	85	°C	-
Input High Voltage	$V_{IH}$	Single-ended inputs, except SMBus.	$0.75 \times V_{DDx}$	-	$V_{DDx} + 0.3$	V	-
Input Low Voltage	$V_{IL}$		-0.3	-	$0.25 \times V_{DDx}$	V	-
Input High Voltage	$V_{IHtri}$	Single-ended tri-level inputs ('_tri' suffix).	$0.8 \times V_{DDx}$	-	$V_{DDx} + 0.3$	V	-
Input Mid Voltage	$V_{IMtri}$		$0.4 \times V_{DDx}$	$0.5 \times V_{DDx}$	$0.6 \times V_{DDx}$	V	-
Input Low Voltage	$V_{ILtri}$		-0.3	-	$0.20 \times V_{DDx}$	V	-

**Table 6. Input/Supply/Common Parameters – Normal Operating Conditions (Cont.)**

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit	Notes
Input Current	$I_{IN}$	Single-ended inputs, $V_{IN} = GND$ , $V_{IN} = V_{DD}$ .	-5	-0.05	5	$\mu A$	-
	$I_{INP}$	Single-ended inputs. $V_{IN} = 0V$ ; inputs with internal pull-up resistors. $V_{IN} = V_{DD}$ ; inputs with internal pull-down resistors.	-50	7	50	$\mu A$	-
Input Frequency	$F_{IN}$	XTAL or X1 input.	-	25	-	MHz	4
Pin Inductance	$L_{pin}$		-	-	7	nH	1
Capacitance	$C_{IN}$	Logic inputs, except DIF_IN.	1.5	-	5	pF	1
	$C_{OUT}$	Output pin capacitance.	-	-	6	pF	1
CLK Stabilization	$t_{STAB}$	From $V_{DD}$ power-up and after input clock stabilization or deassertion of PD# to 1st clock.	-	0.3	1.8	ms	1,2
SS Modulation Frequency	$f_{MOD}$	Triangular modulation.	30	31.6	33	kHz	1
OE# Latency	$t_{LATO\#}$	DIF start after OE# assertion. DIF stop after OE# deassertion.	1	2	3	clocks	1,3
Tdrive_PD#	$t_{DRVPD}$	DIF output enable after PD# de-assertion.	-	-	300	$\mu s$	1,3
Fall Time	$t_F$	Fall time of single-ended control inputs.	-	-	5	ns	1,2
Rise Time	$t_R$	Rise time of single-ended control inputs.	-	-	5	ns	1,2

<sup>1</sup> Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup> Control input must be monotonic from 20% to 80% of input swing.

<sup>3</sup> Time from deassertion until outputs are > 200mV.

<sup>4</sup> Contact the factory for other frequencies.

**Table 7. Differential Low-Power HCSL Outputs**

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit	Notes
Slew Rate	$Trf$	Scope averaging on, fast setting.	2	2.7	4	V/ns	2,3
		Scope averaging, slow setting.	1	1.9	3	V/ns	2,3
Crossing Voltage (abs)	$V_{cross\_abs}$	Scope averaging off.	250	409	550	mV	1,4,5
Crossing Voltage (var)	$\Delta-V_{cross}$	Scope averaging off.	-	14	140	mV	1,4,9
Avg. Clock Period Accuracy	$T_{PERIOD\_AVG}$	9FGL0xxx devices have 0 ppm synthesis error. The maximum occurs with -0.5% SSC.	0	0	+2500	ppm	2,10,12,13
Absolute Period	$T_{PERIOD\_ABS}$	Includes jitter and spread spectrum modulation.	9.95	10	10.0503	ns	2,6
Jitter, Cycle to Cycle	$t_{j\text{cyc-cyc}}$		-	16	50	ps	2
Voltage High	$V_{HIGH}$	Statistical measurement on single-ended signal using oscilloscope math function (scope averaging on).	660	761	850	mV	1
Voltage Low	$V_{LOW}$		-150	-7	150	mV	1

**Table 7. Differential Low-Power HCSL Outputs (Cont.)**

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit	Notes
Absolute Maximum Voltage	$V_{MIN}$	Measurement on single-ended signal using absolute value (scope averaging off).	-	819	1150	mV	1,7,15
Absolute Minimum Voltage	$V_{MAX}$		-300	-46	-		1,8,15
Duty Cycle	$t_{DC}$		45	49	55	%	2
Slew Rate Matching	$\Delta Trf$	Single-ended measurement.	-	6	20	%	1,14
Skew, Output to Output	$t_{sk3}$	Averaging on, $V_T = 50\%$ .	-	12	50	ps	2

<sup>1</sup> Measured from single-ended waveform.

<sup>2</sup> Measured from differential waveform.

<sup>3</sup> Measured from -150 mV to +150 mV on the differential waveform (derived from REFCLK+ minus REFCLK-). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero crossing.

<sup>4</sup> Measured at crossing point where the instantaneous voltage value of the rising edge of REFCLK+ equals the falling edge of REFCLK-.

<sup>5</sup> Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.

<sup>6</sup> Defines as the absolute minimum or maximum instantaneous period. This includes cycle to cycle jitter, relative ppm tolerance, and spread spectrum modulation.

<sup>7</sup> Defined as the maximum instantaneous voltage including overshoot.

<sup>8</sup> Defined as the minimum instantaneous voltage including undershoot.

<sup>9</sup> Defined as the total variation of all crossing voltages of Rising REFCLK+ and Falling REFCLK-. This is the maximum allowed variance in  $V_{CROSS}$  for any particular system.

<sup>10</sup> Refer to Section 8.6.2 of the PCI Express Base Specification, Revision 5.0 for information regarding PPM considerations.

<sup>11</sup> System board compliance measurements must use the test load. REFCLK+ and REFCLK- are to be measured at the load capacitors  $C_L$ . Single-ended probes must be used for measurements requiring single ended measurements. Either single-ended probes with math or differential probe can be used for differential measurements. Test load  $C_L = 2pF$ .

<sup>12</sup> PCIe Gen1 through Gen4 specify  $\pm 300ppm$  frequency tolerances. PCIe Gen5 reduces the allowable tolerance to  $\pm 100ppm$  without spread spectrum.

<sup>13</sup> "ppm" refers to parts per million and is a DC absolute period accuracy specification. 1ppm is 1/1,000,000th of 100.000000MHz exactly or 100Hz. For 100ppm, then we have an error budget of  $100Hz/ppm \times 100ppm = 10kHz$ . The period is to be measured with a frequency counter with measurement window set to 100ms or greater. The  $\pm 100ppm$  applies to systems that do not employ Spread Spectrum clocking, or that use common clock source. For systems employing Spread Spectrum clocking, there is an additional 2,500ppm nominal shift in maximum period resulting from the 0.5% down spread resulting in a maximum average period specification of +2,600ppm for Common Clock architectures. Separate Reference Clock architectures may have a lower allowed spread percentage.

<sup>14</sup> Matching applies to rising edge rate for REFCLK+ and falling edge rate for REFCLK-. It is measured using a  $\pm 75$  mV window centered on the median cross point where REFCLK+ rising meets REFCLK- falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of REFCLK+ should be compared to the Fall Edge Rate of REFCLK-; the maximum allowed difference should not exceed 20% of the slowest edge rate.

<sup>15</sup> At default SMBus amplitude settings.

**Table 8. 12kHz–20MHz Phase Jitter of Differential Outputs**

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Phase Jitter, 12kHz–20MHz	$t_{jph12k20M}$	Differential outputs when device is set to PCIe SRnS mode (Byte1[4:3] = 00).	-	1.9	2	ps (rms)

**Table 9. Current Consumption – 9FGL02**

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit	Notes
Operating Supply Current	I <sub>DDAOP</sub>	V <sub>DDA</sub> , all outputs active at 100MHz.	-	13	17	mA	-
	I <sub>DDOP</sub>	All V <sub>DD</sub> , except V <sub>DDA</sub> , all outputs active at 100MHz.	-	18	23	mA	-
Wake-on-LAN Current (Power down state and Byte 3, bit 5 = '1')	I <sub>DDAPD</sub>	V <sub>DDA</sub> , DIF outputs off, REF output running.	-	0.9	1.5	mA	1
	I <sub>DDPD</sub>	All V <sub>DD</sub> , except V <sub>DDA</sub> , DIF outputs off, REF output running.	-	5.7	8	mA	1
Power Down Current (Power down state and Byte 3, bit 5 = '0')	I <sub>DDAPD</sub>	V <sub>DDA</sub> , all outputs off.	-	0.9	1.5	mA	-
	I <sub>DDPD</sub>	All V <sub>DD</sub> , except V <sub>DDA</sub> , all outputs off.	-	1.7	2.5	mA	-

<sup>1</sup> This is the current required to have the REF output running in Wake-on-LAN mode (Byte 3, bit 5 = 1).

**Table 10. Current Consumption – 9FGL04**

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit	Notes
Operating Supply Current	I <sub>DDAOP</sub>	V <sub>DDA</sub> , all outputs active at 100MHz.	-	13	17	mA	-
	I <sub>DDOP</sub>	All other V <sub>DD</sub> , except V <sub>DDA</sub> , all outputs active at 100MHz.	-	30	39	mA	-
Wake-on-LAN Current (Power down state and Byte 3, bit 5 = '1')	I <sub>DDAPD</sub>	V <sub>DDA</sub> , DIF outputs off, REF output running.	-	0.9	1.5	mA	1
	I <sub>DDPD</sub>	All other V <sub>DD</sub> , except V <sub>DDA</sub> , DIF outputs off, REF output running.	-	5.9	8.0	mA	1
Power Down Current (Power down state and Byte 3, bit 5 = '0')	I <sub>DDAPD</sub>	V <sub>DDA</sub> , all outputs off.	-	0.9	1.5	mA	-
	I <sub>DDPD</sub>	All other V <sub>DD</sub> , except V <sub>DDA</sub> , all outputs off.	-	1.5	2.5	mA	-

<sup>1</sup> This is the current required to have the REF output running in Wake-on-LAN mode (Byte 3, bit 5 = 1).

**Table 11. Current Consumption – 9FGL06**

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit	Notes
Operating Supply Current	I <sub>DDAOP</sub>	V <sub>DDA</sub> , all outputs active at 100MHz.	-	14	17	mA	-
	I <sub>DDOP</sub>	All V <sub>DD</sub> , except V <sub>DDA</sub> and V <sub>DDIO</sub> , all outputs active at 100MHz.	-	16	20	mA	-
	I <sub>DDIOOP</sub>	V <sub>DDIO</sub> , all outputs active at 100MHz.	-	27	32	mA	-
Wake-on-LAN Current (Power down state and Byte 3, bit 5 = '1')	I <sub>DDAPD</sub>	V <sub>DDA</sub> , DIF outputs off, REF output running.	-	0.9	1.5	mA	1
	I <sub>DDPD</sub>	All V <sub>DD</sub> , except V <sub>DDA</sub> and V <sub>DDIO</sub> , DIF outputs off, REF output running.	-	6	8	mA	1
	I <sub>DDIOOP</sub>	V <sub>DDIO</sub> , DIF outputs off, REF output running.	-	0.04	0.05	mA	1

**Table 11. Current Consumption – 9FGL06**

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit	Notes
Power Down Current (Power down state and Byte 3, bit 5 = '0')	I <sub>DDAPD</sub>	V <sub>DDA</sub> , all outputs off.	-	0.9	1.5	mA	-
	I <sub>DDPD</sub>	All V <sub>DD</sub> , except V <sub>DDA</sub> and V <sub>DDIO</sub> , all outputs off.	-	1.8	2.5	mA	-
	I <sub>DDIOOP</sub>	V <sub>DDIO</sub> , all outputs off.	-	0.04	0.08	mA	-

<sup>1</sup> This is the current required to have the REF output running in Wake-on-LAN mode (Byte 3, bit 5 = 1).

**Table 12. Current Consumption – 9FGL08**

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit	Notes
Operating Supply Current	I <sub>DAAOP</sub>	V <sub>DDA</sub> , all outputs active at 100MHz.	-	14	19	mA	-
	I <sub>DDOP</sub>	All V <sub>DD</sub> , except V <sub>DDA</sub> and V <sub>DDIO</sub> , all outputs active at 100MHz.	-	18	24	mA	-
	I <sub>DDIOOP</sub>	V <sub>DDIO</sub> , all outputs active at 100MHz.	-	30	37	mA	-
Wake-on-LAN Current (Power down state and Byte 3, bit 5 = '1')	I <sub>DDAPD</sub>	V <sub>DDA</sub> , DIF outputs off, REF output running.	-	0.9	1.5	mA	1
	I <sub>DDPD</sub>	All V <sub>DD</sub> , except V <sub>DDA</sub> and V <sub>DDIO</sub> , DIF outputs off, REF output running.	-	5.2	8	mA	1
	I <sub>DDIOOP</sub>	V <sub>DDIO</sub> , DIF outputs off, REF output running.	-	0.04	0.1	mA	1
Power Down Current (Power down state and Byte 3, bit 5 = '0')	I <sub>DDAPD</sub>	V <sub>DDA</sub> , all outputs off.	-	0.9	1.5	mA	-
	I <sub>DDPD</sub>	All V <sub>DD</sub> , except V <sub>DDA</sub> and V <sub>DDIO</sub> , all outputs off.	-	1.7	2.3	mA	-
	I <sub>DDIOOP</sub>	V <sub>DDIO</sub> , all outputs off.	-	0.04	0.1	mA	-

<sup>1</sup> This is the current required to have the REF output running in Wake-on-LAN mode (Byte 3, bit 5 = 1).

**Table 13. PCIe Phase Jitter of Differential Outputs**

T<sub>AMB</sub> = over the specified operating range. Supply voltages per normal operation conditions. See [Test Loads](#) for loading conditions.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Limit	Unit	Notes
PCIe Phase Jitter (Common Clocked Architecture)	t <sub>jphPCIeG1-CC</sub>	PCIe Gen1 (2.5 GT/s)	-	18	28	86	ps (p-p)	1,2,7
	t <sub>jphPCIeG2-CC</sub>	PCIe Gen2 Hi Band (5.0 GT/s)	-	0.9	1.6	3	ps (RMS)	1,2,7
		PCIe Gen2 Lo Band (5.0 GT/s)	-	0.4	0.6	3.1	ps (RMS)	1,2,
	t <sub>jphPCIeG3-CC</sub>	PCIe Gen3 (8.0 GT/s)	-	0.25	0.4	1	ps (RMS)	1,2,3,7
	t <sub>jphPCIeG4-CC</sub>	PCIe Gen4 (16.0 GT/s)	-	0.25	0.4	0.5	ps (RMS)	1,2,3,4,7
t <sub>jphPCIeG5-CC</sub>	PCIe Gen5 (32.0 GT/s)	-	0.09	0.11	0.15	ps (RMS)	1,2,3,5,7	
PCIe Phase Jitter (SRIS Architecture)	t <sub>jphPCIeG1-SRIS</sub>	PCIe Gen1 (2.5 GT/s)	-	4	6	N/A	ps (RMS)	1,2,6,8
	t <sub>jphPCIeG2-SRIS</sub>	PCIe Gen2 (5.0 GT/s)	-	0.8	1.1		ps (RMS)	1,2,6,8
	t <sub>jphPCIeG3-SRIS</sub>	PCIe Gen3 (8.0 GT/s)	-	0.3	0.4		ps (RMS)	1,2,6,8
	t <sub>jphPCIeG4-SRIS</sub>	PCIe Gen4 (16.0 GT/s)	-	0.3	0.35		ps (RMS)	1,2,6,8
	t <sub>jphPCIeG5-SRIS</sub>	PCIe Gen5 (32.0 GT/s)	-	0.15	0.19		ps (RMS)	1,2,6,8

- <sup>1</sup> The REFCLK jitter is measured after applying the filter functions found in PCI Express Base Specification 5.0, Revision 1.0. See the [Test Loads](#) section of the data sheet for the exact measurement setup. Values for the Common Clock architecture are calculated for CC/SRIS spread off and spread on at -0.5%. SRIS values are calculated for CC/SRIS spread off and spread on at  $\leq -0.3\%$ . If oscilloscope data is used, equipment noise is removed from all results.
- <sup>2</sup> Jitter measurements shall be made with a capture of at least 100,000 clock cycles captured by a real-time oscilloscope (RTO) with a sample rate of 20 GS/s or greater. Broadband oscilloscope noise must be minimized in the measurement. The measured PP jitter is used (no extrapolation) for RTO measurements. Alternately, jitter measurements may be used with a Phase Noise Analyzer (PNA) extending (flat) and integrating and folding the frequency content up to an offset from the carrier frequency of at least 200MHz (at 300MHz absolute frequency) below the Nyquist frequency. For PNA measurements for the 2.5 GT/s data rate, the RMS jitter is converted to peak to peak jitter using a multiplication factor of 8.83. In the case where real-time oscilloscope and PNA measurements have both been done and produce different results, the RTO result must be used.
- <sup>3</sup> SSC spurs from the fundamental and harmonics are removed up to a cutoff frequency of 2MHz taking care to minimize removal of any non-SSC content.
- <sup>4</sup> Note that 0.7ps RMS is to be used in channel simulations to account for additional noise in a real system.
- <sup>5</sup> Note that 0.25ps RMS is to be used in channel simulations to account for additional noise in a real system.
- <sup>6</sup> While the PCI Express Base Specification 5.0, Revision 1.0 provides the filters necessary to calculate SRIS jitter values, it does not provide specification limits, hence the N/A in the "Limit" column. SRIS values are informative only. In general, a clock operating in an SRIS system must be twice as good as a clock operating in a Common Clock system. For RMS values, twice as good is equivalent to dividing the CC value by  $\sqrt{2}$ . An additional consideration is the value for which to divide by  $\sqrt{2}$ . The conservative approach is to divide the ref clock jitter limit, and the case can be made for dividing the channel simulation values by  $\sqrt{2}$ , if the ref clock is close to the Tx clock input. An example for Gen4 is as follows. A "rule-of-thumb" SRIS limit would be either  $0.5\text{ps RMS}/\sqrt{2} = 0.35\text{ps RMS}$ , or  $0.7\text{ps RMS}/\sqrt{2} = 0.5\text{ps RMS}$ .
- <sup>7</sup> Calculated for Byte1[4:3] spread settings of 01, 10 and 11.
- <sup>8</sup> Calculated for Byte1[4:3] spread settings of 01, and 10.

**Table 14. REF Output**

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit	Notes
Long Accuracy	ppm	See T <sub>period</sub> min-max values.	0			ppm	1,2
Clock Period	T <sub>period</sub>	REF output.	40			ns	2
High Output Voltage	V <sub>HIGH</sub>	I <sub>OH</sub> = -2mA.	0.8 × V <sub>DDREF</sub>	-	-	V	-
Low Output Voltage	V <sub>LOW</sub>	I <sub>OL</sub> = 2mA.	-	-	0.2 × V <sub>DDREF</sub>	V	-
Rise/Fall Slew Rate	t <sub>rf1</sub>	Byte 3 = 1F, V <sub>OH</sub> = 0.8 × V <sub>DD</sub> , V <sub>OL</sub> = 0.2 × V <sub>DD</sub> .	0.5	0.9	1.5	V/ns	1
	t <sub>rf1</sub>	Byte 3 = 5F, V <sub>OH</sub> = 0.8 × V <sub>DD</sub> , V <sub>OL</sub> = 0.2 × V <sub>DD</sub> .	1.0	1.5	2.5	V/ns	1,3
	t <sub>rf1</sub>	Byte 3 = 9F, V <sub>OH</sub> = 0.8 × V <sub>DD</sub> , V <sub>OL</sub> = 0.2 × V <sub>DD</sub> .	1.5	2.1	3.1	V/ns	1
	t <sub>rf1</sub>	Byte 3 = DF, V <sub>OH</sub> = 0.8 × V <sub>DD</sub> , V <sub>OL</sub> = 0.2 × V <sub>DD</sub> .	2.0	2.7	3.8	V/ns	1
Duty Cycle	d <sub>t1X</sub>	V <sub>T</sub> = V <sub>DD</sub> /2 V.	45	49.7	55	%	1,4
Jitter, Cycle to Cycle	t <sub>j<sub>cyc-cyc</sub></sub>	V <sub>T</sub> = V <sub>DD</sub> /2 V.	-	35	125	ps	1,4
Noise Floor	t <sub>jdBc1k</sub>	1kHz offset.	-	-145	-135	dBc	1,4
	t <sub>jdBc10k</sub>	10kHz offset to Nyquist.	-	-150	-140	dBc	1,4
Jitter, Phase	t <sub>j<sub>phREF</sub></sub>	12kHz to 5MHz, DIF SSC off.	-	0.13	0.3	ps (rms)	1,4
		12kHz to 5MHz, DIF SSC on.	-	1.4	1.5	ps (rms)	1,4,5

<sup>1</sup> Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup> All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REF is trimmed to 25.00MHz.

<sup>3</sup> Default SMBus value.

<sup>4</sup> When driven by a crystal.

<sup>5</sup> Does not apply to the 9FGL06x1 devices.

## Power Management

**Table 15. Power Management** <sup>3</sup>

CKPWRGD_PD#	SMBus OE bit	OEx# Pin	Differential Output		REF
			True O/P	Comp. O/P	
0	X	X	Low <sup>1</sup>	Low <sup>1</sup>	Hi-Z <sup>2</sup>
1	1	0	Running	Running	Running
1	1	1	Disabled <sup>1</sup>	Disabled <sup>1</sup>	Running
1	0	X	Disabled <sup>1</sup>	Disabled <sup>1</sup>	Disabled <sup>4</sup>

<sup>1</sup> The output state is set by B11[1:0] (Low/Low default).

<sup>2</sup> REF is Hi-Z until the 1st assertion of CKPWRGD\_PD# high. After this, when CKPWRGD\_PD# is low, REF is disabled unless Byte3[5] = 1, in which case REF is running.

<sup>3</sup> Input polarities defined at default values.

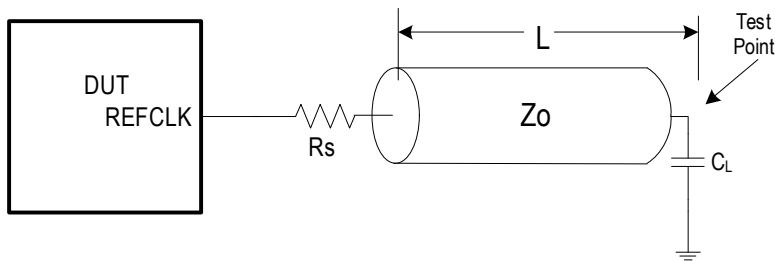
<sup>4</sup> See SMBus description for Byte 3, bit 4.

**Table 16. SMBus Address Selection**

	SADR	Address	+ Read/Write Bit
State of SADR on first application of CKPWRGD_PD#	0	1101000	X
	1	1101010	X

## Test Loads

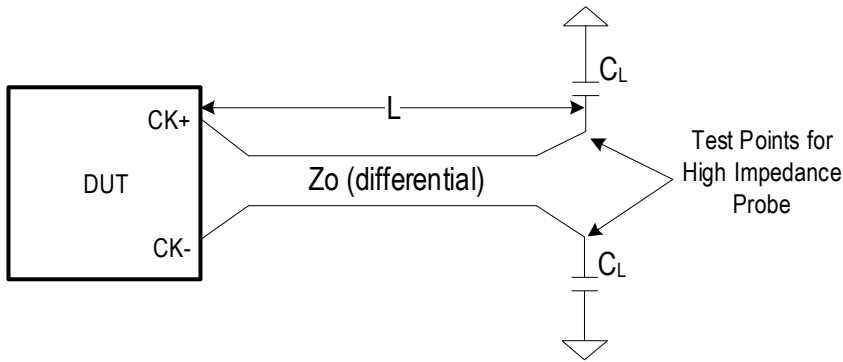
**Figure 5. Single-ended Output Test Load**



**Table 17. Terminations for Single-ended Output**

Clock Source	Device Under Test (DUT)	Rs (Ω)	Zo (Ω)	L (cm)	CL (pF)
N/A	9FGL0nxx	33	50	12.7	4.7

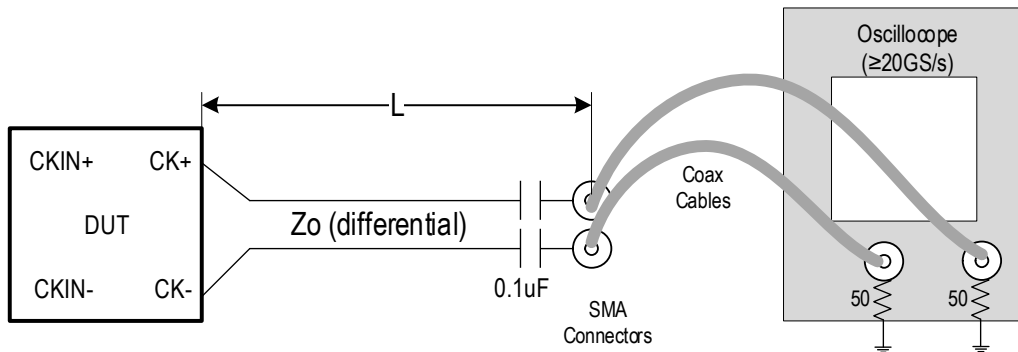
**Figure 6. Test Load for AC/DC Measurements**



**Table 18. Terminations for AC/DC Measurements**

Clock Source	Device Under Test (DUT)	Rs ( $\Omega$ )	Zo ( $\Omega$ )	L (cm)	CL (pF)
N/A	9FGL0x41	Internal	100	12.7	2
N/A	9FGL0x51	Internal	85	12.7	2

**Figure 7. Test Setup for PCIe Clock Phase Jitter Measurements**



**Table 19. Terminations for PCIe Clock Phase Jitter Measurements**

Clock Source	Device Under Test (DUT)	Rs ( $\Omega$ )	Zo ( $\Omega$ )	L (cm)	CL (pF)
N/A	9FGL0x41	Internal	100	12.7	N/A
N/A	9FGL0x51	Internal	85	12.7	N/A

## Alternate Terminations

The 9FGL family can easily drive LVPECL, LVDS, and CML logic. See [“AN-891 Driving LVPECL, LVDS, and CML Logic with “Universal” Low-Power HCSL Outputs”](#) for details.

## Crystal Characteristics

**Table 20. Recommended Crystal Characteristics**

Parameter	Value	Units
Frequency <sup>1</sup>	25	MHz
Resonance Mode	Fundamental	—
Frequency Tolerance at 25°C	±20	ppm maximum
Frequency Stability, reference at 25°C over operating temperature range	±20	ppm maximum
Temperature Range (industrial)	-40 to +85	°C
Temperature Range (commercial)	0 to +70	°C
Equivalent Series Resistance (ESR)	50	Ω maximum
Shunt Capacitance (C <sub>O</sub> )	7	pF maximum
Load Capacitance (C <sub>L</sub> )	8	pF maximum
Drive Level	0.1	mW maximum
Aging per year	±5	ppm maximum

<sup>1</sup> When driven by an external oscillator via the XIN/CLKIN\_25 pin, X2 should be floating.

## General SMBus Serial Interface Information

### How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- Renesas clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- Renesas clock will **acknowledge**
- Controller (host) sends the byte count = X
- Renesas clock will **acknowledge**
- Controller (host) starts sending Byte N through Byte N+X-1
- Renesas clock will **acknowledge** each byte **one at a time**
- Controller (host) sends a stop bit

Index Block Write Operation		
Controller (Host)		Renesas (Slave/Receiver)
T	starT bit	
Slave Address		
WR	WRite	
		ACK
Beginning Byte = N		
		ACK
Data Byte Count = X		
		ACK
Beginning Byte N		
		ACK
0	X Byte	0
0		0
0		0
		0
Byte N + X - 1		
		ACK
P	stoP bit	

Note: Address is latched on SADR pin.

### How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- Renesas clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- Renesas clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- Renesas clock will **acknowledge**
- Renesas clock will send the data byte count = X
- Renesas clock sends Byte N+X-1
- Renesas clock sends **Byte 0 through Byte X (if X<sub>(H)</sub> was written to Byte 8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Read Operation		
Controller (Host)		Renesas
T	starT bit	
Slave Address		
WR	WRite	
		ACK
Beginning Byte = N		
		ACK
RT	Repeat starT	
Slave Address		
RD	ReaD	
		ACK
		Data Byte Count=X
ACK		
		Beginning Byte N
ACK		
0	X Byte	0
0		0
0		0
0		0
		Byte N + X - 1
N	Not acknowledge	
P	stoP bit	

**Table 21. Byte 0: Output Enable Register**

Byte 0 <sup>1</sup>	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
<b>Control Function</b>	Output Enable	Output Enable	Output Enable	Output Enable	Output Enable	Output Enable	Output Enable	Output Enable
<b>Type</b>	RW	RW	RW	RW	RW	RW	RW	RW
<b>0</b>	See B11[1:0]							
<b>1</b>	OE# Pin Controls Output							
<b>9FGL08 Name</b>	OE7	OE6	OE5	OE4	OE3	OE2	OE1	OE0
<b>9FGL08 Default</b>	1	1	1	1	1	1	1	1
<b>9FGL06 Name</b>	OE5	OE4	Reserved	OE3	OE2	OE1	Reserved	OE0
<b>9FGL06 Default</b>	1	1	x	1	1	1	x	1
<b>9FGL04 Name</b>	Reserved	Reserved	Reserved	Reserved	OE3	OE2	OE1	OE0
<b>9FGL04 Default</b>	x	x	x	x	1	1	1	1
<b>9FGL02 Name</b>	Reserved	Reserved	Reserved	Reserved	Reserved	OE1	OE0	Reserved
<b>9FGL02 Default</b>	x	x	x	x	x	1	1	x

<sup>1</sup> A low on these bits will override the OE# pin and force the differential output to the state indicated by B11[1:0] (Low/Low default)

**Table 22. Byte 1: Spread Spectrum with V<sub>HIGH</sub> Control Register**

Byte 1	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
<b>Control Function</b>	SS Enable Readback Bit1	SS Enable Readback Bit0	Enable software control of spread spectrum	SS Software Control Bit1	SS Software Control Bit0	Reserved	Controls Output Amplitude	
<b>Type</b>	R	R	RW	RW <sup>1</sup>	RW <sup>1</sup>		RW	RW
<b>0</b>	See <a href="#">Spread Selection</a> table		SS controlled by latch (B1[7:6])	See <a href="#">Spread Selection</a> table			00 = 0.6V	10 = 0.75V
<b>1</b>			Values in B1[4:3] control SS amount				01 = 0.68V	11 = 0.85V
<b>Name</b>	SSENRB1	SSENRB1	SSEN_SWCNTRL	SSENSW1	SSENSW0		AMPLITUDE 1	AMPLITUDE 0
<b>Default</b>	Latch	Latch	0	0	0	x	1	0

<sup>1</sup> See notes on [Spread Selection](#) table. B1[5] must be set to a 1 in order to use B1[4:3].

**Table 23. Byte 2: DIF Slew Selection Register**

Byte 2	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
<b>Control Function</b>	Select fast or slow slew rate	Select fast or slow slew rate	Select fast or slow slew rate	Select fast or slow slew rate	Select fast or slow slew rate	Select fast or slow slew rate	Select fast or slow slew rate	Select fast or slow slew rate
<b>Type</b>	RW	RW	RW	RW	RW	RW	RW	RW
<b>0</b>	Slow Slew Rate							
<b>1</b>	Fast Setting							
<b>9FGL08 Name</b>	DIF7_slew	DIF6_slew	DIF5_slew	DIF4_slew	DIF3_slew	DIF2_slew	DIF1_slew	DIF0_slew
<b>9FGL08 Default</b>	1	1	1	1	1	1	1	1
<b>9FGL06 Name</b>	DIF5_slew	DIF4_slew	Reserved	DIF3_slew	DIF2_slew	DIF1_slew	Reserved	DIF0_slew
<b>9FGL06 Default</b>	1	1	x	1	1	1	x	1
<b>9FGL04 Name</b>	Reserved	Reserved	Reserved	Reserved	DIF3_slew	DIF2_slew	DIF1_slew	DIF0_slew
<b>9FGL04 Default</b>	x	x	x	x	1	1	1	1
<b>9FGL02 Name</b>	Reserved	Reserved	Reserved	Reserved	Reserved	DIF1_slew	DIF0_slew	Reserved
<b>9FGL02 Default</b>	x	x	x	x	x	1	1	x

<sup>1</sup> See [Differential Low-Power HCSL Outputs](#) table for slew rates.

**Table 24. Byte 3: REF Slew Rate Control Register**

Byte 3	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
<b>Control Function</b>	Slew Rate Control		Wake-on-Lan Enable for REF	REF Output Enable	Reserved	Reserved	Reserved	Reserved
<b>Type</b>	RW	RW	RW	RW				
<b>0</b>	00 = Slowest	10 = Fast	REF disabled in Power Down	Disabled <sup>1</sup>				
<b>1</b>	01 = Slow	11 = Fastest	REF runs in Power Down	Enabled				
<b>Name</b>	REF Slew Rate [1:0]		REF Power Down Function	REF OE				
<b>Default</b>	0	1	0	1	x	x	x	x

<sup>1</sup> The disabled state depends on Byte11[1:0]. '00' = Low, '01' = HiZ, '10' = Low, '11' = High.

**Byte 4 is Reserved**

**Table 25. Byte 5: Revision and Vendor ID Register**

Byte 5	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Control Function	Revision ID				VENDOR ID			
Type	R	R	R	R	R	R	R	R
0	C rev = 0010				0001 = Renesas			
1								
Name	RID3	RID2	RID1	RID0	VID3	VID2	VID1	VID0

**Table 26. Byte 6: Device Type/Device ID Register**

Byte 6	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Control Function	Device Type		Device ID					
Type	R	R	R	R	R	R	R	R
0	00 = FGL		9FGL08 = 0b00100 9FGL06 = 0b00110 9FGL04 = 0b00100 9FGL02 = 0b00010					
1								
Name	Device Type1	Device Type0	Device ID5	Device ID4	Device ID3	Device ID2	Device ID1	Device ID0

**Table 27. Byte 7: Byte Count Register**

Byte 7	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Control Function	Reserved	Reserved	Reserved	Byte Count Programming				
Type				RW	RW	RW	RW	RW
0				Writing to this register will configure how many bytes will be read back.				
1								
Name				BC4	BC3	BC2	BC1	BC0
Default	x	x	x	0	1	0	0	0

Bytes 8 and 9 are Reserved

**Table 28. Byte 10: PLL MN Enable, PD\_Restore Register**

Byte 10	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
<b>Control Function</b>	M/N Programming Enable	Restore Default Config. In PD	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
<b>Type</b>	RW	RW						
<b>0</b>	M/N Prog. Disabled	Clear Config in PD						
<b>1</b>	M/N Prog. Enabled	Keep Config in PD						
<b>Name</b>	PLL M/N En	Power-Down (PD) Restore						
<b>Default</b>	0	1	x	x	x	x	x	x

**Table 29. Byte 11: Stop State Control Register**

Byte 11	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
<b>Control Function</b>	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	True/Complement DIF Output Disable State	
<b>Type</b>							RW	RW
<b>0</b>							00 = Low/Low	01 = HiZ/HiZ
<b>1</b>							10 = High/Low	11 = Low/High
<b>Name</b>							STP[1]	STP[0]
<b>Default</b>	x	x	x	x	x	x	0	0

**Table 30. Byte 12: Impedance Control Register 1**

Byte 12	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
<b>Control Function</b>	Output impedance control [1:0]		Output impedance control [1:0]		Output impedance control [1:0]		Output impedance control [1:0]	
<b>Type</b>	RW	RW	RW	RW	RW	RW	RW	RW
<b>0</b>	00 = 33ohm DIF Zout, 01 = 85ohm DIF Zout							
<b>1</b>	10 = 100ohm DIF Zout, 11 = Reserved							
<b>9FGL08 Name</b>	DIF3_imp[1]	DIF3_imp[0]	DIF2_imp[1]	DIF2_imp[0]	DIF1_imp[1]	DIF1_imp[0]	DIF0_imp[1]	DIF0_imp[0]
<b>9FGL08 Default</b>	9FGL0841 defaults to 0b10101010 9FGL0851 defaults to 0b01010101							
<b>9FGL06 Name</b>	DIF2_imp[1]	DIF2_imp[0]	DIF1_imp[1]	DIF1_imp[0]	Reserved	Reserved	DIF0_imp[1]	DIF0_imp[0]
<b>9FGL06 Default</b>	9FGL0641 defaults to 0b1010xx10 9FGL0651 defaults to 0b0101xx01							
<b>9FGL04 Name</b>	DIF1_imp[1]	DIF1_imp[0]	Reserved	Reserved	DIF0_imp[1]	DIF0_imp[0]	Reserved	Reserved

**Table 30. Byte 12: Impedance Control Register 1 (Cont.)**

Byte 12	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
9FGL04 Default	9FGL0441 defaults to 0b10xx10xx 9FGL0451 defaults to 0b01xx01xx							
9FGL02 Name	DIF0_imp[1]	DIF0_imp[0]	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
9FGL02 Default	9FGL0241 defaults to 0b10xxxxxx 9FGL0251 defaults to 0b01xxxxxx							

**Table 31. Byte 13: Impedance Control Register 2**

Byte 13	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Control Function	Output impedance control [1:0]		Output impedance control [1:0]		Output impedance control [1:0]		Output impedance control [1:0]	
Type	RW	RW	RW	RW	RW	RW	RW	RW
0	00 = 33ohm DIF Zout, 01 = 85ohm DIF Zout							
1	10 = 100ohm DIF Zout, 11 = Reserved							
9FGL08 Name	DIF7_imp[1]	DIF7_imp[0]	DIF6_imp[1]	DIF6_imp[0]	DIF5_imp[1]	DIF5_imp[0]	DIF4_imp[1]	DIF4_imp[0]
9FGL08 Default	9FGL0841 defaults to 0hAA 9FGL0851 defaults to 0h55							
9FGL06 Name	DIF5_imp[1]	DIF5_imp[0]	DIF4_imp[1]	DIF4_imp[0]	Reserved	Reserved	DIF3 Zout	DIF3 Zout
9FGL06 Default	9FGL0641 defaults to 0b1010xx10 9FGL0651 defaults to 0b0101xx01							
9FGL04 Name	Reserved	Reserved	DIF3_imp[1]	DIF3_imp[0]	DIF2_imp[1]	DIF2_imp[0]	Reserved	Reserved
9FGL04 Default	9FGL0441 defaults to 0bxx1010xx 9FGL0451 defaults to 0bxx0101xx							
9FGL02 Name	Reserved	Reserved	Reserved	Reserved	DIF1_imp[1]	DIF1_imp[0]	Reserved	Reserved
9FGL02 Default	9FGL0241 defaults to 0bxxxx10xx 9FGL0251 defaults to 0bxxxx01xx							

**Table 32. Byte 14: Pull-up Pull-down Control Register 1**

Byte 14	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
<b>Control Function</b>	Pull-up(pu)/ Pull-down(pd) control		Pull-up(pd)/ Pull-down(pd) control		Pull-up(pd)/ Pull-down(pd) control		Pull-up(pd)/ Pull-down(pd) control	
<b>Type</b>	RW	RW	RW	RW	RW	RW	RW	RW
<b>0</b>	00 = None	01 = pd	00 = None	01 = pd	00 = None	01 = pd	00 = None	01 = pd
<b>1</b>	10 = pu	11 = pu+pd	10 = pu	11 = pu+pd	10 = pu	11 = pu+pd	10 = pu	11 = pu+pd
<b>9FGL08 Name</b>	OE3_pu/pd[1]	OE3_pu/pd[0]	OE2_pu/pd[1]	OE2_pu/pd[0]	OE1_pu/pd[1]	OE1_pu/pd[0]	OE0_pu/pd[1]	OE0_pu/pd[0]
<b>9FGL08 Default</b>	0	1	0	1	0	1	0	1
<b>9FGL06 Name</b>	OE2_pu/pd[1]	OE2_pu/pd[0]	OE1_pu/pd[1]	OE1_pu/pd[0]	Reserved	Reserved	OE0_pu/pd[1]	OE0_pu/pd[0]
<b>9FGL06 Default</b>	0	1	0	1	x	x	0	1
<b>9FGL04 Name</b>	OE1_pu/pd[1]	OE1_pu/pd[0]	Reserved	Reserved	OE0_pu/pd[1]	OE0_pu/pd[0]	Reserved	Reserved
<b>9FGL04 Default</b>	0	1	x	x	0	1	x	x
<b>9FGL02 Name</b>	OE0_pu/pd[1]	OE0_pu/pd[0]	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
<b>9FGL02 Default</b>	0	1	x	x	x	x	x	x

**Table 33. Byte 15: Pull-up Pull-down Control Register 2**

Byte 15	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
<b>Control Function</b>	Pull-up(pd)/ Pull-down(pd) control		Pull-up(pd)/ Pull-down(pd) control		Pull-up(pd)/ Pull-down(pd) control		Pull-up(pd)/ Pull-down(pd) control	
<b>Type</b>	RW	RW	RW	RW	RW	RW	RW	RW
<b>0</b>	00 = None	01 = pd	00 = None	01 = pd	00 = None	01 = pd	00 = None	01 = pd
<b>1</b>	10 = pu	11 = pu+pd	10 = pu	11 = pu+pd	10 = pu	11 = pu+pd	10 = pu	11 = pu+pd
<b>9FGL08 Name</b>	OE7_pu/pd[1]	OE7_pu/pd[0]	OE6_pu/pd[1]	OE6_pu/pd[0]	OE5_pu/pd[1]	OE5_pu/pd[0]	OE4_pu/pd[1]	OE4_pu/pd[0]
<b>9FGL08 Default</b>	0	1	0	1	0	1	0	1
<b>9FGL06 Name</b>	OE5_pu/pd[1]	OE5_pu/pd[0]	OE4_pu/pd[1]	OE4_pu/pd[0]	Reserved	Reserved	OE3_pu/pd[1]	OE3_pu/pd[0]
<b>9FGL06 Default</b>	0	1	0	1	0	1	0	1
<b>9FGL04 Name</b>	Reserved	Reserved	OE3_pu/pd[1]	OE3_pu/pd[0]	OE2_pu/pd[1]	OE2_pu/pd[0]	Reserved	Reserved

**Table 33. Byte 15: Pull-up Pull-down Control Register 2 (Cont.)**

Byte 15	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
9FGL04 Default	0	1	0	1	0	1	0	1
9FGL02 Name	Reserved	Reserved	Reserved	Reserved	OE1_pu/pd[1]	OE1_pu/pd[0]	Reserved	Reserved
9FGL02 Default	0	1	0	1	0	1	0	1

**Table 34. Byte 16: Pull-up Pull-down Control Register 3**

Byte 16	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Control Function	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Pull-up(pd)/ Pull-down(pd) control	
Type							RW	RW
0							00 = None	01 = pd
1							10 = pu	11 = pu+pd
Name							CKPWRGD_ PD_pu/pd[1]	CKPWRGD_ PD_pu/pd[0]
Default	0	0	1	0	0	1	1	0

Byte 17 is Reserved

**Table 35. Byte 18: Polarity Control Register 2**

Byte 18	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
<b>Control Function</b>	Sets OE pin polarity	Sets OE pin polarity	Sets OE pin polarity	Sets OE pin polarity	Sets OE pin polarity	Sets OE pin polarity	Sets OE pin polarity	Sets OE pin polarity
<b>Type</b>	RW	RW	RW	RW	RW	RW	RW	RW
<b>0</b>	Output enabled when OE pin is low							
<b>1</b>	Output enabled when OE pin is high							
<b>9FGL08 Name</b>	OE7_polarity	OE6_polarity	OE5_polarity	OE4_polarity	OE3_polarity	OE2_polarity	OE1_polarity	OE0_polarity
<b>9FGL08 Default</b>	0	0	0	0	0	0	0	0
<b>9FGL06 Name</b>	OE5_polarity	OE4_polarity	Reserved	OE3_polarity	OE2_polarity	OE1_polarity	Reserved	OE0_polarity
<b>9FGL06 Default</b>	0	0	0	0	0	0	0	0
<b>9FGL04 Name</b>	Reserved	OE3_polarity	OE2_polarity	Reserved	OE1_polarity	Reserved	OE0_polarity	Reserved
<b>9FGL04 Default</b>	0	0	0	0	0	0	0	0
<b>9FGL02 Name</b>	Reserved	Reserved	OE1_polarity	Reserved	OE0_polarity	Reserved	Reserved	Reserved
<b>9FGL02 Default</b>	0	0	0	0	0	0	0	0

**Table 36. Byte 19: Polarity Control Register 1**

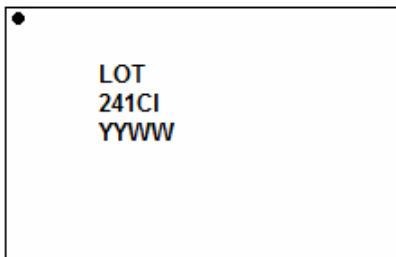
Byte 19	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
<b>Control Function</b>	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Sets CKPWRGD_PD polarity
<b>Type</b>								RW
<b>0</b>								Power Down when Low
<b>1</b>								Power Down when High
<b>Name</b>								CKPWRGD_PD_polarity
<b>Default</b>								0

## Package Outline Drawings

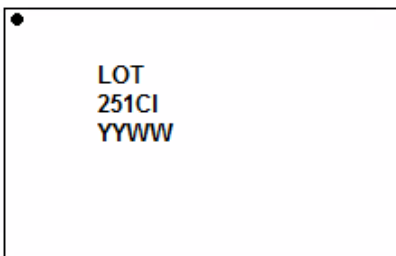
The package outline drawings are located at the end of this document and are accessible from the Renesas website (see [Ordering Information](#) for POD links). The package information is the most current data available and is subject to change without revision of this document.

## Marking Diagrams

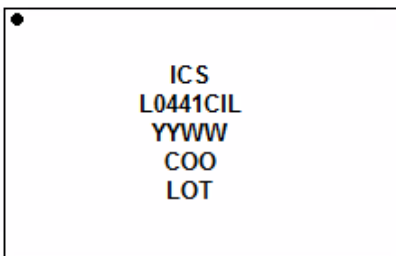
### 9FGL02



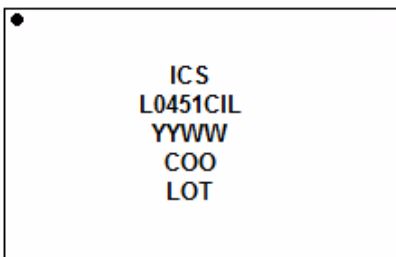
- Line 1: "LOT" denotes the lot number.
- Line 2: truncated part number.
- Line 3: "YYWW" is the last two digits of the year and the work week the part was assembled.



### 9FGL04



- Lines 1 and 2: truncated part number
- Line 3: "YYWW" is the last two digits of the year and the work week the part was assembled.
- Line 4: "COO" denotes country of origin.
- Line 5: "LOT" denotes the lot number.



### 9FGL06

•  
ICS  
GL0641CI  
YYWW  
COO  
LOT

- Lines 1 and 2: truncated part number
- Line 3: "YYWW" is the last two digits of the year and the work week the part was assembled.
- Line 4: "COO" denotes country of origin.
- Line 5: "LOT" denotes the lot number.

•  
ICS  
GL0651CI  
YYWW  
COO  
LOT

### 9FGL08

•  
ICS  
FGL0841CI  
YYWW  
COO  
LOT

- Lines 1 and 2: truncated part number
- Line 3: "YYWW" is the last two digits of the year and the work week the part was assembled.
- Line 4: "COO" denotes country of origin.
- Line 5: "LOT" denotes the lot number.

•  
ICS  
FGL0851CI  
YYWW  
COO  
LOT

## Ordering Information

**Table 37. Ordering Information**

Number of Clock Outputs	Output Impedance	Part Number	Package	Temperature Range	Part Number Suffix and Shipping Method
2	100	9FGL0241CKILF	24-VFQFPN	-40°C to +85°C	None = Trays "T" = Tape and Reel, Pin 1 Orientation: EIA-481C (see Table 38 for more details)
		9FGL0241CKILFT			
	85	9FGL0251CKILF			
		9FGL0251CKILFT			
4	100	9FGL0441CKILF	32-VFQFPN		
		9FGL0441CKILFT			
	85	9FGL0451CKILF			
		9FGL0451CKILFT			
6	100	9FGL0641CKILF	40-VFQFPN		
		9FGL0641CKILFT			
	85	9FGL0651CKILF			
		9FGL0651CKILFT			
8	100	9FGL0841CKILF	48-VFQFPN		
		9FGL0841CKILFT			
	85	9FGL0851CKILF			
		9FGL0851CKILFT			

"C" is the device revision designator (will not correlate with the datasheet revision).

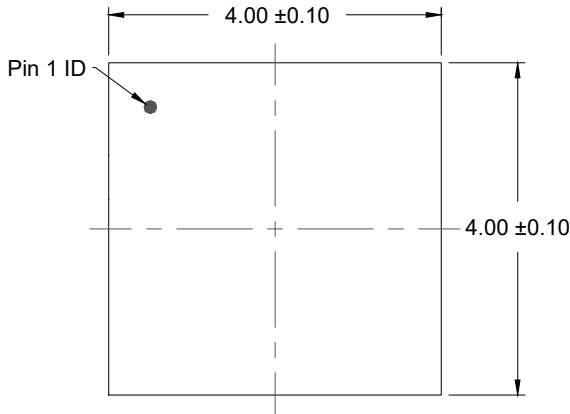
"LF" denotes Pb-free configuration, RoHS compliant.

**Table 38. Pin 1 Orientation in Tape and Reel Packaging**

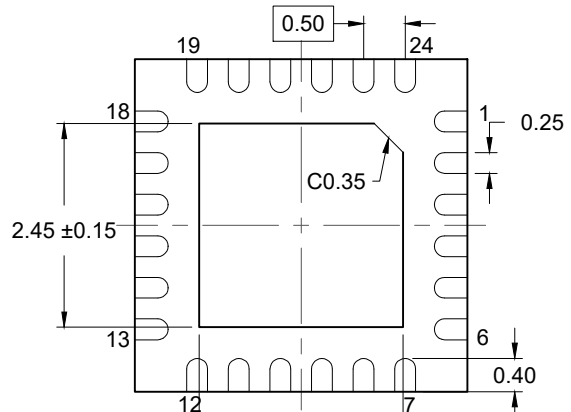
Part Number Suffix	Pin 1 Orientation	Illustration
T	Quadrant 1 (EIA-481-C)	

## Revision History

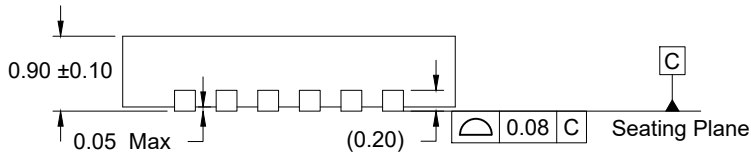
Revision Date	Description of Change
December 1, 2022	Updated POD links in <a href="#">Ordering Information</a> table.
June 2, 2022	<ul style="list-style-type: none"> <li>▪ Updated Input High Voltage, SMBus maximum rating in <a href="#">Absolute Maximum Ratings</a> table.</li> <li>▪ Updated <a href="#">Package Outline Drawings</a> section.</li> </ul>
November 17, 2020	<ul style="list-style-type: none"> <li>▪ Updated DIF5# pin numbers for 9FGL06x1.</li> <li>▪ Rebranded to Renesas.</li> </ul>
October 10, 2019	Initial release.



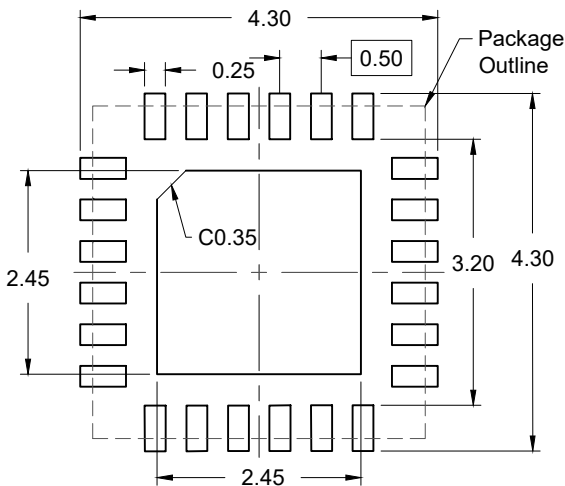
TOP VIEW



BOTTOM VIEW



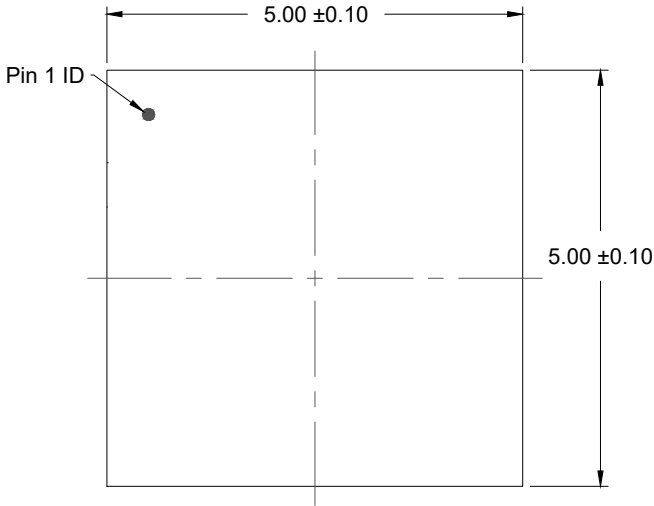
SIDE VIEW



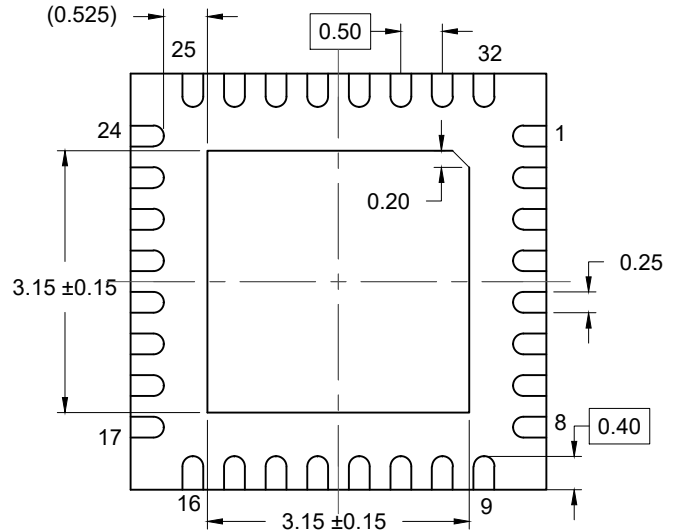
RECOMMENDED LAND PATTERN  
(PCB Top View, NSMD Design)

NOTES:

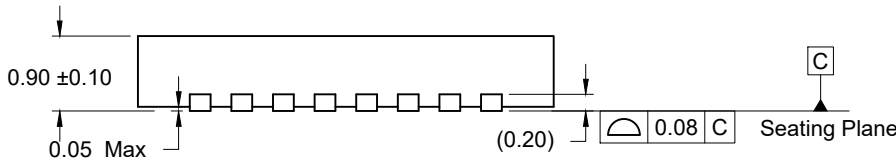
1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use  $\pm 0.05$  mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.



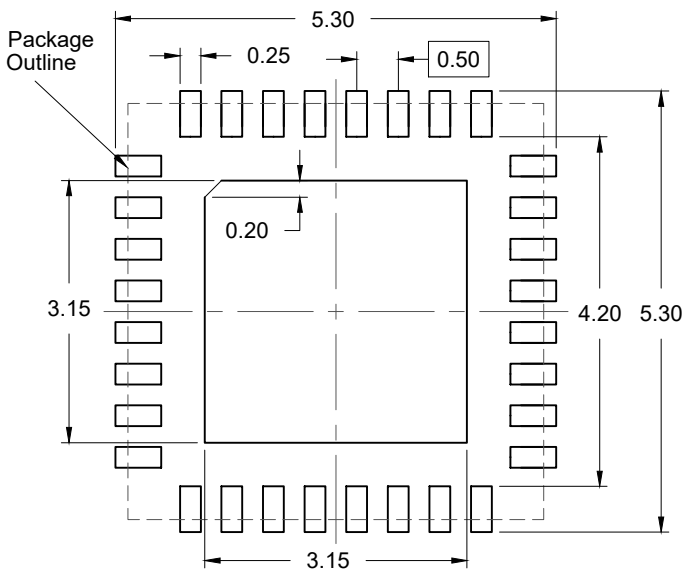
TOP VIEW



BOTTOM VIEW



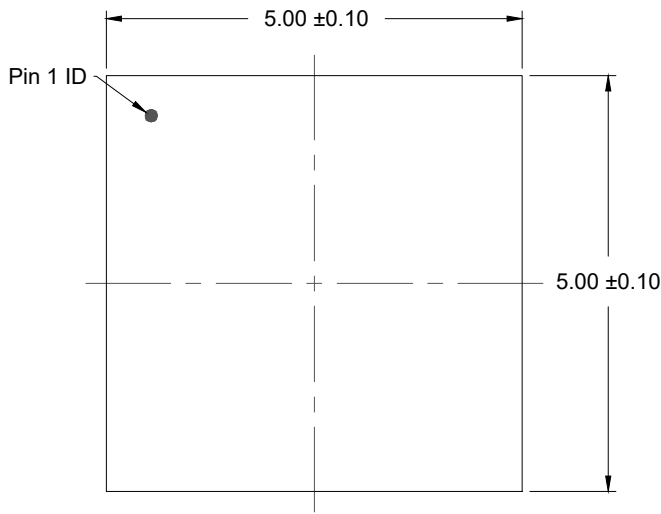
SIDE VIEW



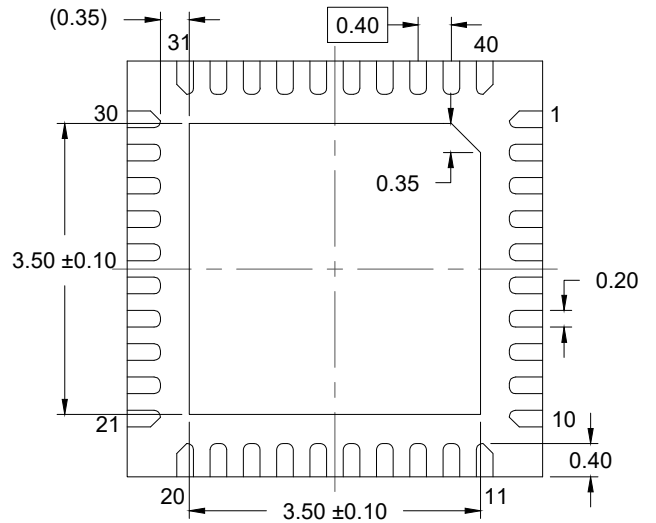
RECOMMENDED LAND PATTERN  
(PCB Top View, NSMD Design)

**NOTES:**

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use  $\pm 0.05$  mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.



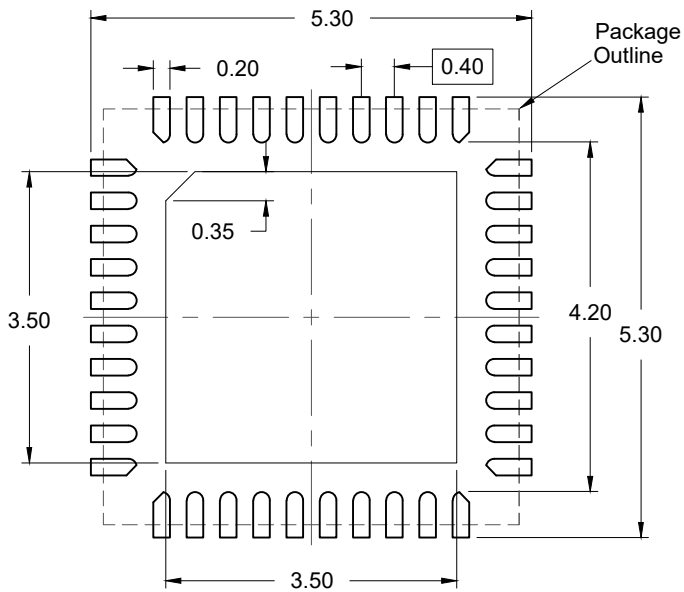
TOP VIEW



BOTTOM VIEW



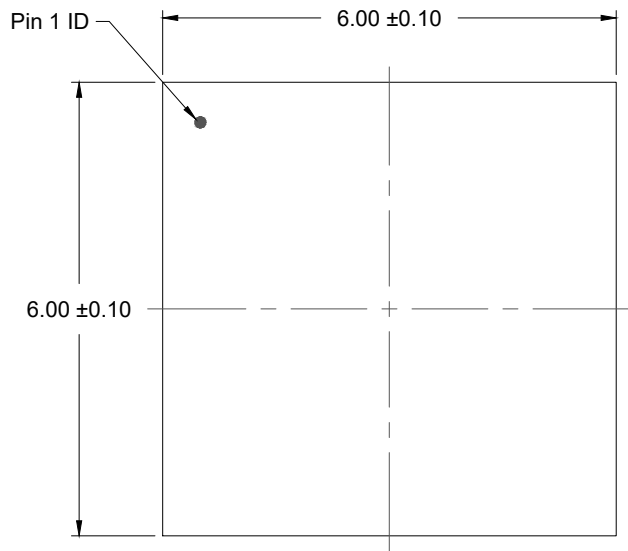
SIDE VIEW



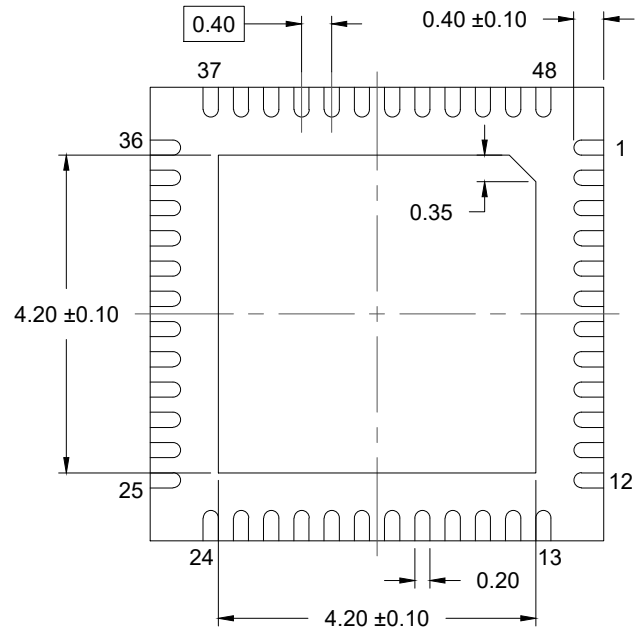
RECOMMENDED LAND PATTERN  
(PCB Top View, NSMD Design)

**NOTES:**

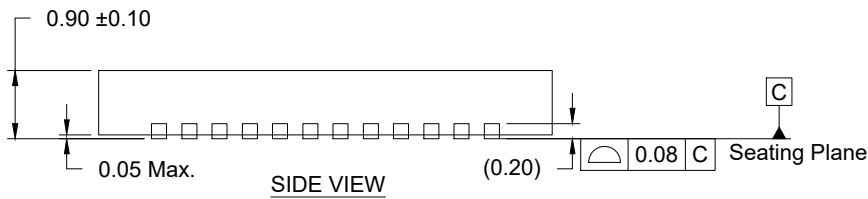
1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use  $\pm 0.05$  mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.



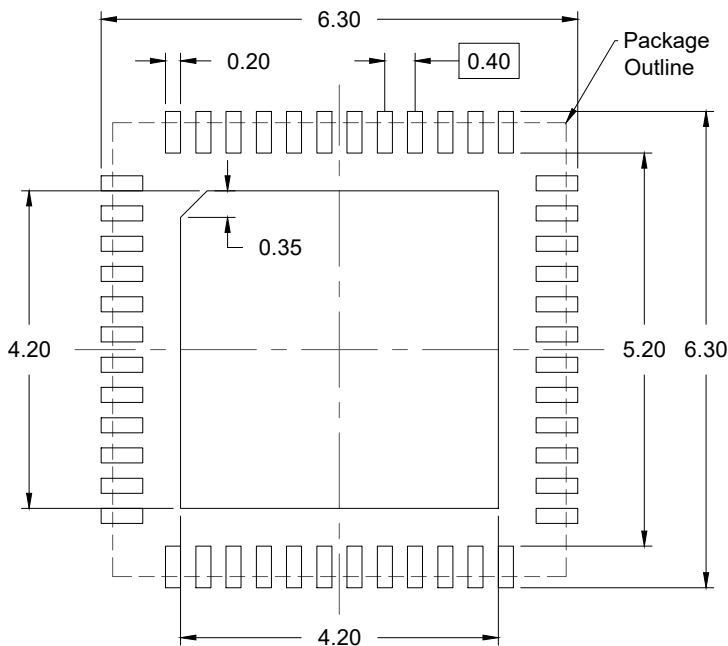
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN  
(PCB Top View, NSMD Design)

NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use  $\pm 0.05$  mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.

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