DLPR410 Configuration PROM

1 特性

- 预编程的 Xilinx® PROM 可配置 DLPC410ZYR DMD 数字控制器
- I/O 引脚电压范围 1.8V 至 3.3V
- 1.8V 内核电源电压
- 工作温度范围：-40°C 至 85°C

2 应用

平版印刷
- 直接成像
- 平板显示器
- 印刷电路板制造

工业类
- 3D 打印
- 用于机器视觉的 3D 扫描仪
- 质量控制

显示器
- 3D 成像
- 智能和自适应照明
- 增强现实和信息覆盖

3 说明

DLPR410 器件是一款经编程的 PROM，用于正确配置 DLPC410ZYR 控制器，从而运行五个不同的数字微镜器件 (DMD) 选件：DLP650LNIRFYL、DLP7000FLP、DLP7000UVFLP、DLP9500FLN 和 DLP9500UVFLN DMD。此器件中的固件使 DLPC410ZYR 控制器能够提供高达 48 千兆位/秒 (Gbps) 的系统数据吞吐量，并提供随机行寻址和 Load4 功能选项。通常，此系列芯片设计用于高速 UV 和 NIR 光学系统，例如需要快速吞吐量和像素精确控制的直接成像平版印刷系统、3D 打印和激光打标设备。

查看 TI DLP® 光控制技术页面，了解如何开始使用 DLPC410ZYR。ti.com 上的 DLP 先进光控制资源可加快上市速度，这些资源包括评估模块、参考设计、光学模块制造商和 DLP 设计网络合作伙伴。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
DLPR410	DSBGA (48)	8.00mm × 9.00mm × 1.20mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

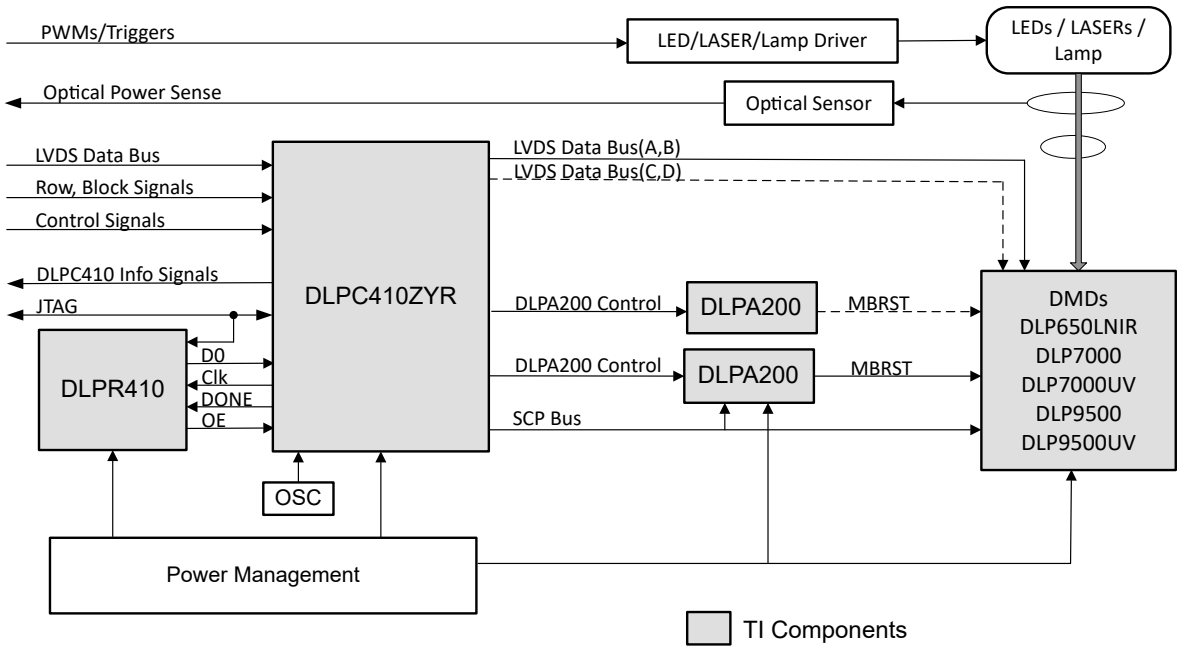

图 3-1. 简化版应用

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision F (January 2020) to Revision G (August 2021) — **Page**

- 将数据表中对 DLPC410 控制器的所有引用更新为 DLPC410ZYR 控制器 1
- 更新了应用列表 1
- 更新了“说明”部分中的简化应用图 1
- 将 Xilinx XCF 规格链接移到“规格”部分顶部 1
- Removed numbers appended to all DNC signals in Pin Functions table 4
- Added entry for V_{CCJ} to Absolute Maximum Ratings 6
- Removed footnote reference to JEDEC Standard JESD22-A114A in ESD Ratings 6
- Added entry for V_{CCJ} to Recommended Operating Conditions 6
- Updated DLPC410ZYR and DLPR410 Connection Schematic 10
- Updated DLPR410 and DLPC410ZYR with DMD Example Block Diagram 11
- Added Application Curves section 12
- Added 0.047-µF decoupling capacitor to GND for all Power Pins in Power Supply Recommendations 13
- Added Layout Example section 14
- Added DLPR410BYVA to Device Compatibility table 15
- Added DLPR410BYVA to Part Number Description table 15
- Added DLPR410B Device Markings 15

Changes from Revision E (December 2018) to Revision F (January 2020) — **Page**

- Corrected Max Tstg per Xilinx data sheet 6
- Pulled in specific layout information from referenced document and removed reference 13
- Corrected DDC_Version(3:0) bus width to DDC_Version(2:0). 15

Changes from Revision D (April 2015) to Revision E (December 2018) — **Page**

- 更新了*应用*和*说明*以包含新的 DLP650LNIR，移除了数据传输速率 1
- Corrected Min Tstg per Xilinx data sheet 6

- Corrected Min VCCO per Xilinx data sheet 6
- Added support information for new DLP650LNIR DMD (multiple places)..... 8
- Updated 节 7.2 8
- Corrected improper "DLPC910" reference to "DLPC410" 11
- Updated 图 8-1 11
- Added 节 11.1.1 table..... 15
- Updated 节 11.1.2 15
- Updated *节 11.1.3* section..... 15
- Added DLP650LNIR to 表 11-2 section..... 17
- Deleted DLP Discovery 4100 Chipset reference in 表 11-2 17

Changes from Revision C (March 2013) to Revision D (October 2015) **Page**

- 更新了*特性*、*应用* 和 *说明* 1
- 通篇删除了 DLPR4101 (增强功能 PROM 器件型号) 1
- 添加了 *ESD 等级*表、*特性说明*部分、*器件功能模式*、*应用和实现*部分、*电源相关建议*部分、*布局*部分、*器件和文档支持*部分以及*机械、封装和可订购信息*部分。 1
- Deleted 1.8 V and 3.3 V operation values from V_{CCO}, V_{IL}, and V_{IH} - this implementation is 2.5 V 6
- Changed Device Marking Image 15
- Changed Device Marking Image 15
- Deleted DLP® Discovery™ 4100 Chipset Datasheet from *Related Documentation* 17
- Added Link to XCF16P data sheet at xilinx.com 17

Changes from Revision B (March 2013) to Revision C (April 2013) **Page**

- 添加了“器件顶视图” 1
- 向“特性”添加了 DLPR4101“Load 4”增强功能..... 1
- 通篇向 DLPR410 添加了 DLPR410 和 DLPR4101 (增强功能 PROM 器件型号) 1
- 添加了指向数据表的链接..... 1
- Added the Version column to the *Ordering Information* table..... 4
- Updated DLPC and DLP7000 / DLP7000UV Embedded Example Block Diagram..... 11
- Added DLP7000UV and DLP9500UV well suited for direct imaging lithography, 3D printing, and UV applications 11
- Added DLPR4101YVA as equivalent to TI part number 2510442-0006 15
- Added Reference to DLPC410 data sheet..... 15
- Added DLPR410 to 图 11-2 15
- Added Top View of Device to device marking 15
- Added DLP7000UV Related Documentation..... 17
- Added DLP9500UV Related Documentation..... 17

Changes from Revision A (September 2012) to Revision B (March 2013) **Page**

- Changed the top-side marking in the *Ordering Information* table..... 4

Changes from Revision * (August 2012) to Revision A (September 2012) **Page**

- 将器件从“产品预发布”更改为“量产” 1

5 Pin Configuration and Functions

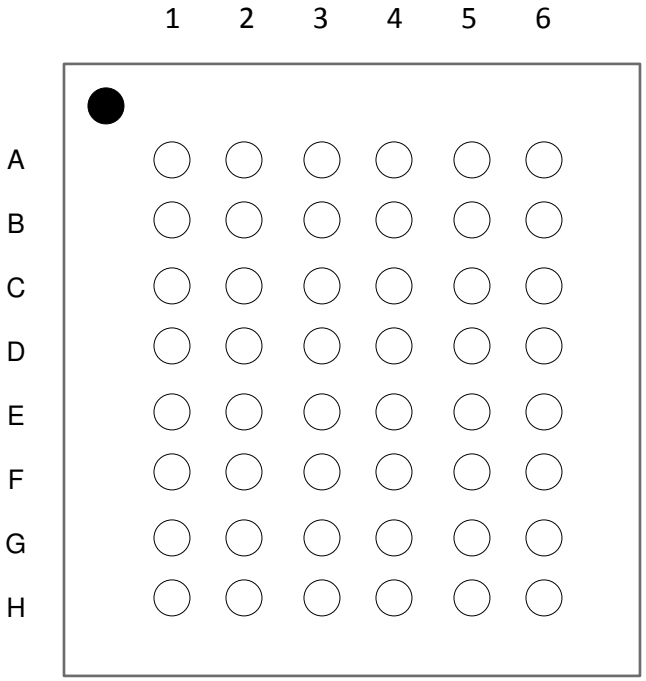

图 5-1. YVA Package 48-Pin DSBGA Top View

表 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
GND	A1	G	Ground
GND	A2	G	Ground
OE/ $\overline{\text{RESET}}$	A3	I/O	Output Enable/ $\overline{\text{RESET}}$ (Open-Drain I/O). When Low, this input holds the address counter reset and the DATA and CLKOUT outputs are placed in a high-impedance state. This is a bidirectional open-drain pin that is held Low while the PROM completes the internal power-on reset sequence. Polarity is not programmable. **Pin must be pulled High using an external 4.7-kΩ pull-up to V_{CCO}.**
DNC	A4	—	Do Not Connect. Leave unconnected.
D6	A5	—	Do Not Connect. Leave unconnected.
D7	A6	—	Do Not Connect. Leave unconnected.
VCCINT1	B1	P	Positive 1.8-V supply voltage for internal logic.
VCCO1	B2	P	Positive supply voltage connected to the output voltage drivers and internal buffers.
CLK	B3	I	Do Not Connect. Leave unconnected.
$\overline{\text{CE}}$	B4	I	Chip Enable Input. When $\overline{\text{CE}}$ is High, the device is put into low-power standby mode, the address counter is reset, and the DATA and CLKOUT outputs are placed in a high impedance state. **Pin must be pulled High using an external 4.7-kΩ pull-up to V_{CCO}.**
D5	B5	—	Do Not Connect. Leave unconnected.
GND	B6	G	Ground
BUSY	C1	—	Do Not Connect. Leave unconnected.
CLKOUT	C2	—	Configuration clock output. Each rising edge on the CLK input increments the internal address counter. **Pin must be pulled High and Low using an external 100-Ω pull-up to V_{CCO} and an external 100-Ω pull-down to Ground. Place resistors close to pin.**
DNC	C3	—	Do Not Connect. Leave unconnected.
DNC	C4	—	Do Not Connect. Leave unconnected.
D4	C5	—	Do Not Connect. Leave unconnected.

表 5-1. Pin Functions (continued)

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
VCCO2	C6	P	Positive supply voltage connected to the output voltage drivers and internal buffers.
$\overline{CF}$	D1	I	Configuration pin. **The $\overline{CF}$ pin must be pulled High using an external 4.7-kΩ pull-up to V_{CCO}.** Selects serial mode configuration.
$\overline{CEO}$	D2	—	Do Not Connect. Leave unconnected.
DNC	D3	—	Do Not Connect. Leave unconnected.
DNC	D4	—	Do Not Connect. Leave unconnected.
D3	D5	—	Do Not Connect. Leave unconnected.
VCCO4	D6	P	Positive supply voltage connected to the output voltage drivers and internal buffers.
VCCINT2	E1	P	Positive 1.8-V supply voltage for internal logic.
TMS	E2	I	JTAG Mode Select Input. TMS has an internal 50-kΩ resistive pull-up to V_{CCJ}.
DNC	E3	—	Do Not Connect. Leave unconnected.
DNC	E4	—	Do Not Connect. Leave unconnected.
DNC	E5	—	Do Not Connect. Leave unconnected.
TDO	E6	O	JTAG Serial Data Output. TDO has an internal 50-kΩ resistive pull-up to V_{CCJ}.
GND	F1	G	Ground
DNC	F2	—	Do Not Connect. Leave unconnected.
DNC	F3	—	Do Not Connect. Leave unconnected.
DNC	F4	—	Do Not Connect. Leave unconnected.
GND	F5	G	Ground
GND	F6	G	Ground
TDI	G1	I	JTAG Serial Data Input. TDI has an internal 50k-Ω resistive pull-up to V_{CCJ}.
DNC	G2	—	Do Not Connect. Leave unconnected.
REV_SEL0	G3	I	Revision Select [1:0] Inputs. When the $\overline{EN\_EXT\_SEL}$ is Low, the Revision Select pins are used to select the design revision to be enabled. The Revision Select [1:0] inputs have an internal 50-kΩ resistive pull-up to V_{CCO}. **The REV_SEL0 pin must be pulled Low using an external 4.7-kΩ pull-down to Ground. The REV_SEL1 pin must be pulled Low using an external 4.7-kΩ pull-down to Ground.**
REV_SEL1	G4	I	
VCCO3	G5	P	Positive supply voltage connected to the output voltage drivers and internal buffers.
VCCINT3	G6	P	Positive 1.8-V supply voltage for internal logic.
GND	H1	G	Ground
VCCJ	H2	P	Positive 2.5-V JTAG I/O supply voltage connected to the TDO output voltage driver and TCK, TMS and TDI input buffers.
TCK	H3	I	JTAG Clock Input. This pin is the JTAG test clock. It sequences the TAP controller and all the JTAG test and programming electronics.
$\overline{EN\_EXT\_SEL}$	H4	I	External Selection Input. $\overline{EN\_EXT\_SEL}$ has an internal 50-kΩ resistive pull- up to V_{CCO}. **The $\overline{EN\_EXT\_SEL}$ pin must be connected to Ground**.
D1	H5	—	Do Not Connect. Leave unconnected.
D0	H6	O	DATA output pin to provide data for configuring the DLPC410ZYR in serial mode.

(1) P = Power, G = Ground, I = Input, O = Output

6 Specifications

For complete electrical and mechanical specifications of the DLPR410, see the XCF16P product specification listed in *Related Documentation*.

6.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted) (see (1) (2))

			MIN	MAX	UNIT
V_{CCINT}	Internal supply voltage	Relative to ground	–0.5	2.7	V
V_{CCO}	I/O supply voltage	Relative to ground	–0.5	4.0	V
V_{CCJ}	JTAG I/O supply voltage	Relative to ground	–0.5	4.0	V
V_{IN}	Input voltage with respect to ground	V_{CCO} < 2.5 V	–0.5	3.6	V
		V_{CCO} ≥ 2.5 V	–0.5	3.6	V
V_{TS}	Voltage applied to high-impedance output	V_{CCO} < 2.5 V	–0.5	3.6	V
		V_{CCO} ≥ 2.5 V	–0.5	3.6	V
T_J	Junction temperature			125	°C
T_{stg}	Storage temperature, ambient		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under 节 6.3 is not implied. Exposure to absolute-maximum-rated conditions for extended periods can affect device reliability.
(2) Maximum DC undershoot below GND must be limited to either 0.5 V or 10 mA. During transitions, the device pins can undershoot to –2 V or overshoot to 7 V, provided this overshoot or undershoot lasts less than 10 ns and with the forcing current being limited to 200 mA.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$ (1)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (2)	2000	V

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges in to the device.
(2) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CCINT}	Internal voltage supply		1.65	1.8	2.0	V
V_{CCO}	Supply voltage for output drivers	2.5-V operation	2.3	2.5	2.7	V
V_{CCJ}	JTAG I/O Supply voltage	2.5-V operation	2.3	2.5	2.7	V
V_{IL}	Low-level input voltage	2.5-V operation	0		0.7	V
V_{IH}	High-level input voltage	2.5-V operation	1.7		3.6	V
V_O	Output voltage		0		V_{CCO}	V
t_{IN}	Input signal transition time (measured between 10% V_{CCO} and 90% V_{CCO})				500	ns
T_A	Operating ambient temperature		–40		85	°C

6.4 Thermal Information

Refer to the XCF16P product specifications.

6.5 Electrical Characteristics

Refer to the XCF16P product specifications at www.xilinx.com.

6.6 Supply Voltage Requirements for Power-On Reset and Power-Down

(see (1))

		MIN	MAX	UNIT
t_{VCC}	V_{CCINT} rise time from 0 V to nominal voltage (2)	0.2	50	ms
V_{CCPOR}	POR threshold for V_{CCINT} supply	0.5	–	V
t_{OER}	OE/ $\overline{\text{RESET}}$ release delay following POR (3)	0.5	30	ms
V_{CCPD}	Power-down threshold for V_{CCINT} supply		0.5	V
t_{RST}	Time required to trigger a device reset when the V_{CCINT} supply drops below the maximum V_{CCPD} threshold	10		ms

(1) V_{CCINT}, V_{CCO}, and V_{CCJ} supplies can be applied in any order.
(2) At power-up, the device requires the V_{CCINT} power supply to monotonically rise to the nominal operating voltage within the specified t_{VCC} rise time. If the power supply cannot meet this requirement, then the device might not perform power-on-reset properly. See Platform Flash PROM Power-Up Requirements, in the Xilinx XCF16P (v2.19) Product Specification for more information.
(3) If the V_{CCINT} and V_{CCO} supplies do not reach their respective recommended operating conditions before the OE/ $\overline{\text{RESET}}$ pin is released, then the configuration data from the PROM is not available at the recommended threshold levels. The configuration sequence must be delayed until both V_{CCINT} and V_{CCO} have reached their recommended operating conditions.

6.7 Timing Requirements

Refer to the XCF16P product specifications at www.xilinx.com.

7 Detailed Description

7.1 Overview

The configuration bit stream stored in the DLPR410 device supports reliable operation of the DLPC410ZYR device with the DLP650LNIRFYL, DLP7000FLP, DLP7000UVFLP, DLP9500FLN and, DLP9500UVFLN DMDs. DMDs. The DLPC410ZYR digital controller loads this configuration bit stream from the DLPR410 device.

7.2 Functional Block Diagram

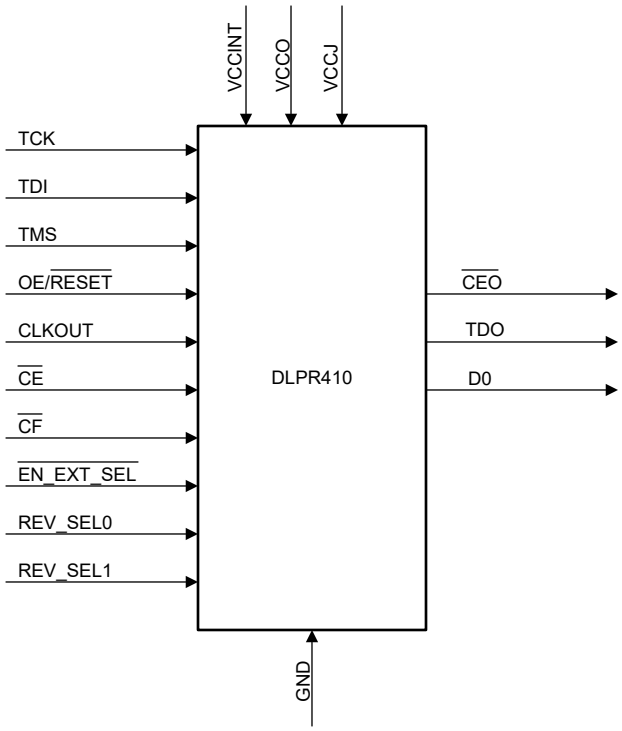

图 7-1. Functional Block Diagram

7.3 Feature Description

7.3.1 Data Interface

7.3.1.1 Data Outputs

The DLPR410 device is configured for serial mode operation, where D0 is the data output pin. D0 output pin provides a serial connection to the DLPC410ZYR controller, where the configuration is read out by the DLPC410ZYR controller.

7.3.1.2 Configuration Clock Input

The configuration CLK is connected to the DLPC410ZYR controller in Primary Serial mode, where the DLPC410ZYR controller provides the clock pulses to read the configuration from the DLPR410 device.

7.3.1.3 Output Enable and Reset

When the OE/ $\overline{\text{RESET}}$ input is held low, the address counter is reset and the Data (D0) and CLKOUT outputs are placed in high-impedance state. **OE/ $\overline{\text{RESET}}$ must be pulled High using an external 4.7-kΩ pull-up to V_{CCO}.**

7.3.1.4 Chip Enable

The $\overline{\text{CE}}$ input is asserted by the DLPC410ZYR controller to enable the Data (D0) and CLKOUT outputs. When $\overline{\text{CE}}$ is held high, the DLPR410 device address counter is reset, and the Data and CLKOUT outputs are placed in high-impedance states.

7.3.1.5 Configuration Pulse

The DLPR410 device is configured in serial mode when it holds configuration pulse pin, $\overline{CF}$, high and it enables the $\overline{CE}$ and OE pins. New data is available a short time after each rising clock edge.

7.3.1.6 Revision Selection

The device uses the REV_SEL0, REV_SEL1, and $\overline{EN\_EXT\_SEL}$ signals to select a revision to act as the default. Setting all three signals to GND defaults to revision 0 for simple DLPR410 device setup.

7.4 Device Functional Modes

To successfully program the DLPC410ZYR controller upon power-up, the DLPR410 device must be configured and connected to the DLPC410ZYR controller as shown in 图 7-2.

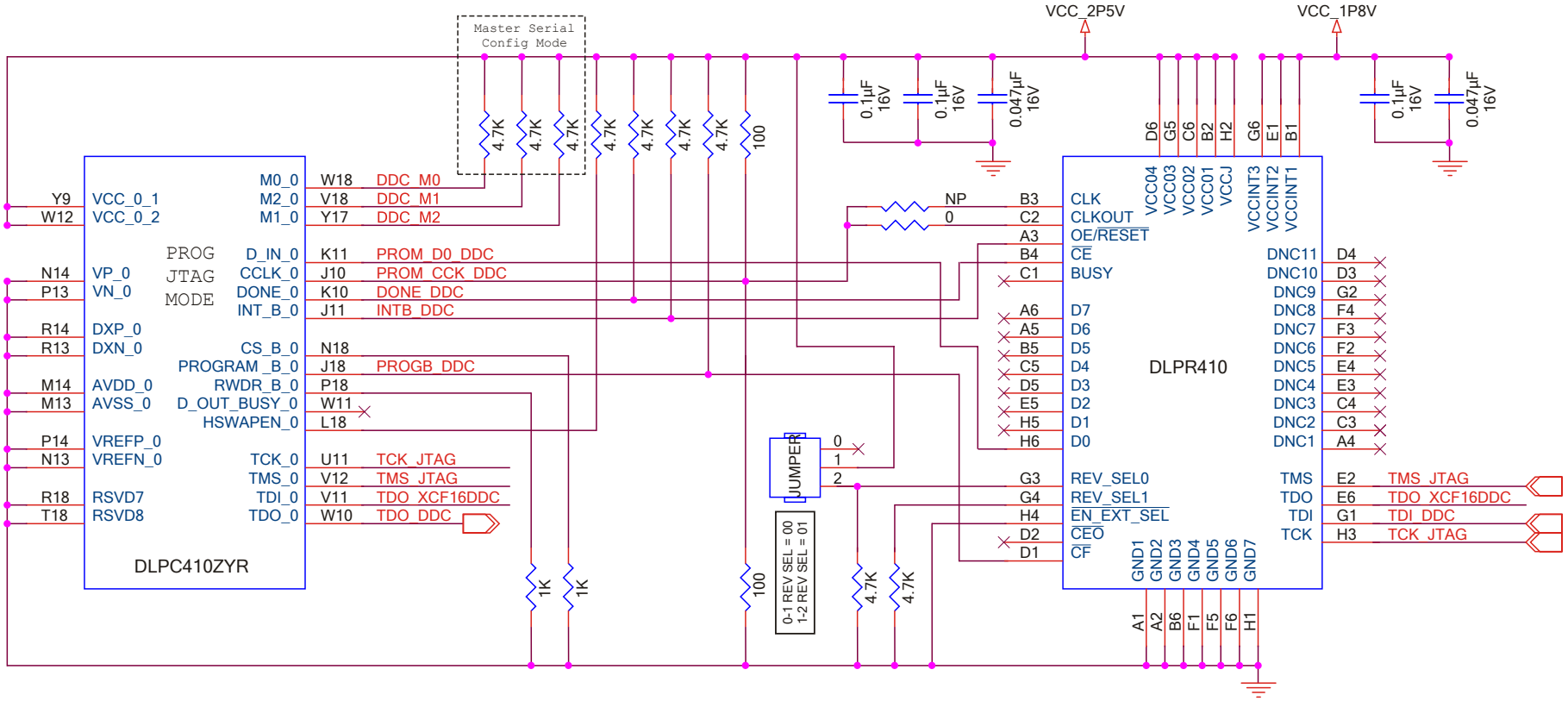

图 7-2. DLPC410ZYR and DLPR410 Connection Schematic

8 Application and Implementation

Note

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

The DLPR410 device configuration PROM ships pre-programmed with configuration code for the DLPC410ZYR controller. Upon power-up, the DLPC410ZYR controller and the DLPR410 device connect to enable configuration information to be sent from the DLPR410 device to the DLPC410ZYR controller, such that the DLPC410ZYR controller can configure itself for proper operation within the application. Without the DLPR410 device properly connected to the DLPC410ZYR controller in the application system, the DLPC410ZYR controller does not boot and the system remains inoperable.

8.2 Typical Application

A typical embedded system application using the DLPR410 device to program the DLPC410 controller (to drive one of 5 different DMDs) is shown in 图 8-1. For complete details of this typical application refer to the DLPC410 controller data sheet listed in *表 11-2*.

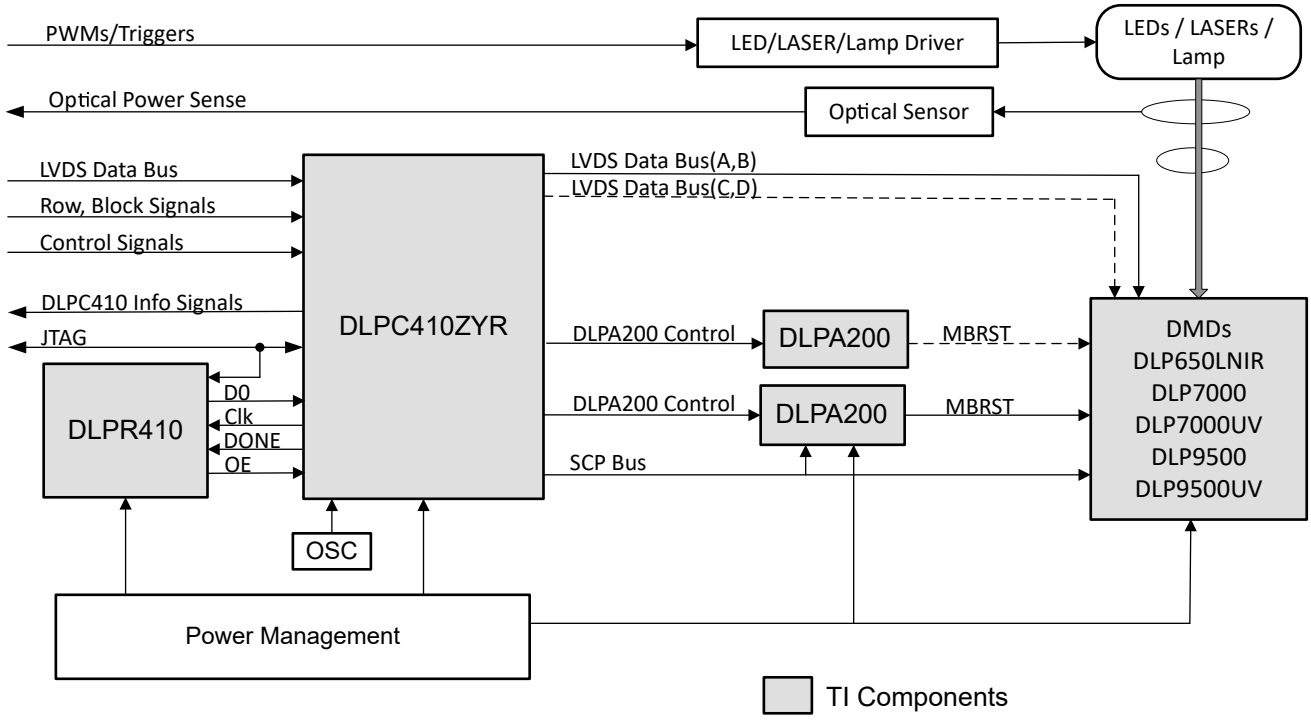

图 8-1. DLPR410 and DLPC410ZYR with DMD Example Block Diagram

8.2.1 Design Requirements

The DLPR410 is part of a multi-chipset solution, and it is required to be coupled with the DLPC410ZYR controller for reliable operation of the DLP650LNIRFYL, DLP7000FLP, DLP7000UVFLP, DLP9500FLN and, DLP9500UVFLN DMDs. DMDs. For more information, refer to the DLPC410ZYR datasheet listed in *节 11.2.1*.

8.2.2 Detailed Design Procedure

The DMDs are designed to be operated by the DLPC410ZYR Digital Controller:

- The DLP7000FLP and DLP9500FLN DMDs are well suited for visible light applications requiring fast, spatially programmable light patterns using the micromirror array.

- The DLP7000UVFLP and DLP9500UVFLN DMDs are well suited for direct imaging lithography, 3D printing applications, and other applications requiring ultraviolet light (UVA).
- The DLP650LNIRFYL DMD enables high-power NIR laser illumination for dynamic digital printing, sintering and marking solutions.

Connections between the DLPC410ZYR Digital Controller, the DLPR410 Configuration PROM, and the DLPA200 DMD micromirror driver(s) must follow the layout guidelines for reliability.

8.2.3 Application Curves

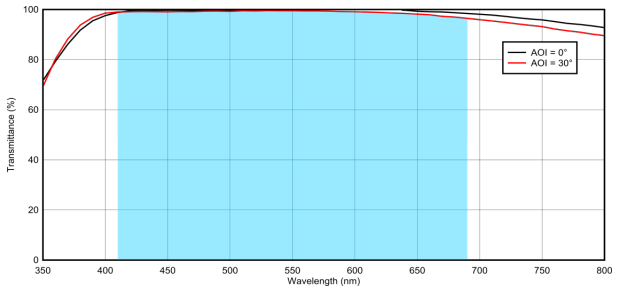

图 8-2. DLP7000 and DLP9500 Transmittance (Visible Window)

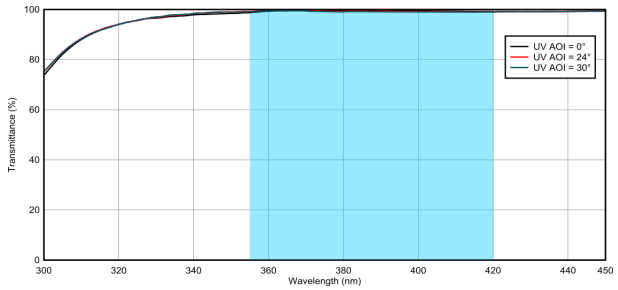

图 8-3. DLP7000UV and DLP9500UV Transmittance (UV Window)

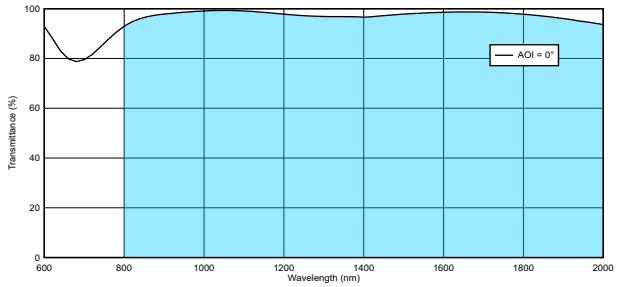

图 8-4. DLP650LNIR Transmittance (NIR Window)

9 Power Supply Recommendations

The DLPR410 uses two power supply rails as shown in 表 9-1.

表 9-1. DLPR410 Power Supply Rails

SUPPLY	POWER PINS	COMMENTS
1.8 V	V_{CCINT1}, V_{CCINT2}, and V_{CCINT3}	All V_{CCINT} pins must be connected with a 0.1-µF and a 0.047- µ F decoupling capacitor to GND.
2.5 V	V_{CCO1},V_{CCO2},V_{CCO3}, V_{CCO4}, and V_{CCJ}	All V_{CCO} and V_{CCJ} pins must be connected with a 0.1-µF and a 0.047- µ F decoupling capacitor to GND.

10 Layout

10.1 Layout Guidelines

The DLPR410 is part of a multi-chipset solution. It is required to be used with the DLPC410ZYR Controller to provide reliable control of any attached DMDs. These guidelines are targeted at designing a PCB board with the DLPR410.

10.1.1 Component Placement

The DLPR410 must be placed adjacent to the DLPC410ZYR Controller with a maximum electrical distance of 4 inches (10 cm).

10.1.2 Impedance Requirements

Signals between the DLPR410 and the DLPC410ZYR Controller must be routed to have a matched impedance of 50 Ω ±10%.

10.1.3 PCB Signal Routing

When designing a PCB board which includes the DLPR410 and the DLPC410ZYR Controller, the following are recommended:

Signal trace corners must be no sharper than 45°. Adjacent signal layers must have the predominate traces routed orthogonal to each other.

TI does not recommend signal routing on power or ground planes.

TI does not recommend ground plane slots.

High speed signal traces must not cross over slots in adjacent power and/or ground planes.

10.1.4 Fiducials

Fiducials for automatic component insertion must be 0.05-inch copper with a 0.1-inch cutout (antipad). Fiducials for optical auto insertion are placed on three corners of both sides of the PCB.

10.1.5 PCB Decoupling Guidelines

Decoupling capacitors must be utilized to provide instantaneous current sources to components and to help mitigate ground bounce.

10.1.5.1 Bulk Decoupling

Bulk decoupling capacitors for the board must be distributed around the PCB and be sized to handle the current demands for the board.

10.1.5.1.1 DLPR410 Decoupling Capacitors

Decoupling capacitors (0.1 µF recommended) are placed to minimize the distance from the decoupling capacitor to the supply and ground pins of the component. It is recommended that the placement of and routing for the decoupling capacitors meet the following guidelines:

- The supply voltage pin of the capacitor must be located close to the device supply voltage pin(s). The decoupling capacitor must have vias to ground and voltage planes. The device can be connected directly to

the decoupling capacitor (no via) if the trace length is less than 0.1 inch. Otherwise, the component must be tied to the voltage or ground plane through separate vias.

- The trace lengths of the voltage and ground connections for decoupling capacitors and components must be less than 0.1 inch to minimize inductance.
- The trace width of the power and ground connection to decoupling capacitors and components must be as wide as possible to minimize inductance.
- Connecting decoupling capacitors to ground and power planes through multiple vias can reduce inductance and improve noise performance. Via sharing between components (discreet or integrated) is discouraged.
- Decoupling performance can be improved by utilizing low ESR and low ESL capacitors.

10.1.6 Layout Example

Please refer to the DLPLCRC410EVM Design files for an example of how to layout the DLPR410 Configuration PROM.

11 Device and Documentation Support

11.1 Device Support

11.1.1 Device Compatibility

TI PART NUMBER	DDC_Version(2:0)(2)	Compatible DMDs (1)
DLPR410YVA	5	DLP7000FLP, DLP7000UVFLP, DLP9500FLN and, DLP9500UVFLN DMDs.
DLPR410AYVA	7	DLP650LNIRFYL, DLP7000FLP, DLP7000UVFLP, DLP9500FLN and, DLP9500UVFLN DMDs.
DLPR410BYVA	0	DLP650LNIRFYL, DLP7000FLP, DLP7000UVFLP, DLP9500FLN and, DLP9500UVFLN DMDs.

(1) Refer to each individual DMD datasheet under Device and Documentation Support for more DMD information.
(2) Refers to the DDC_Version(2:0) output pins of the DLPC410 Controller once configured by this Configuration PROM. See the DLPC410 datasheet (DLPS024) for more information.

11.1.2 Device Nomenclature

The device nomenclature is as shown in 图 11-1. The part number description for previously and currently available part numbers is shown in 表 11-1.

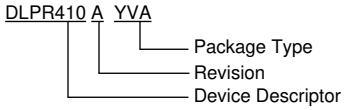

图 11-1. Device Nomenclature

表 11-1. Part Number Description

TI PART NUMBER	DESCRIPTION	REFERENCE NUMBER
DLPR410YVA	DLPR410 Configuration PROM	2510442-0005
DLPR410AYVA	DLPR410A Configuration PROM (Added compatibility with DLP650LNIR)	DLPR410AYVA
DLPR410BYVA	DLPR410B Configuration PROM (Compatibile with DLP650LNIR)	DLPR410BYVA

11.1.3 Device Markings

图 11-2 shows the previous device marking for the DLPR410 device. For the DLPR410A and DLPR410B, this device marking nomenclature has been updated to use the DLPR410A and DLPR410B device part numbers instead of the previous 2510442 marking, as shown in 图 11-3 and 图 11-4.

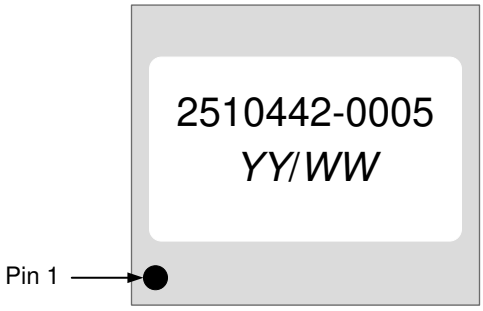

图 11-2. DLPR410 Device Markings

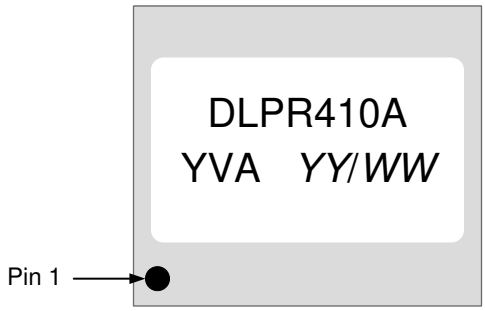

图 11-3. DLPR410A Device Markings

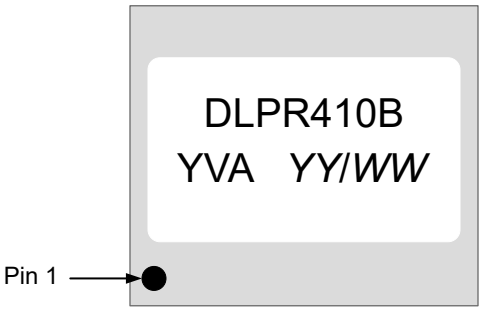

图 11-4. DLPR410B Device Markings

Where *YY*/*WW* is the year/week the part was programmed.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation, see the following:

表 11-2. Related Documentation

DOCUMENT	TI LITERATURE NUMBER
DLP650LNIR 0.65 NIR WXGA S450 DMD data sheet	DLPS136
DLP7000 DLP 0.7 XGA 2xLVDS Type A DMD data sheet	DLPS026
DLP7000UV DLP 0.7 UV XGA 2xLVDS Type-A DMD data sheet	DLPS061
DLP9500 DLP 0.95 1080p 2xLVDS Type-A DMD data sheet	DLPS025
DLP9500UV DLP 0.95 UV 1080p 2xLVDS Type-A DMD data sheet	DLPS033
DLPA200 DMD Micromirror Driver data sheet	DLPS015
DLPC410 DMD Digital Controller data sheet	DLPS024
XCF16P data sheet	available at www.xilinx.com

11.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this datasheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DLPR410AYVA	ACTIVE	DSBGA	YVA	48	3	TBD	Call TI	Call TI	-40 to 85		Samples
DLPR410BYVA	LIFEBUY	DSBGA	YVA	48	3	TBD	Call TI	Call TI	-40 to 85		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

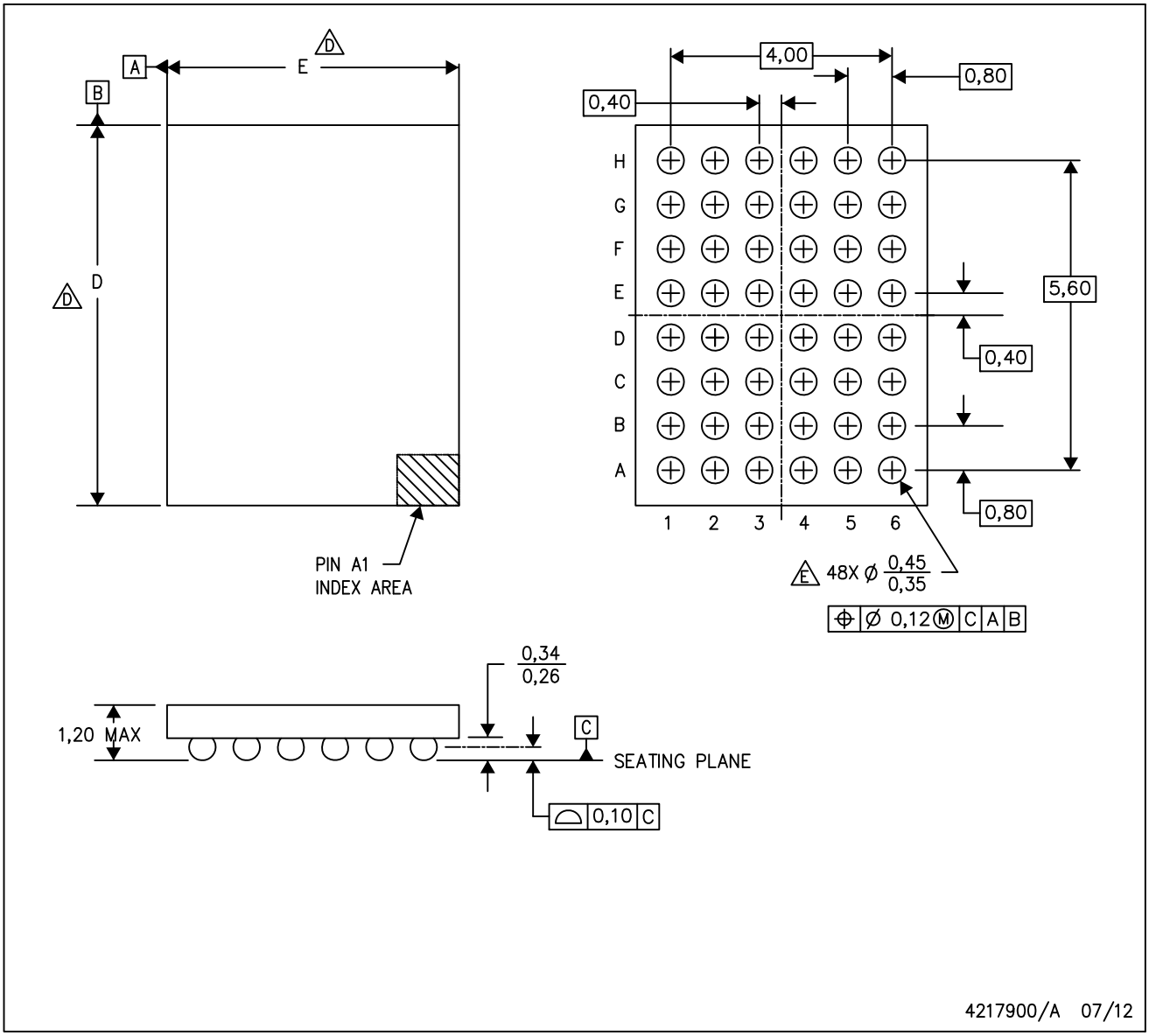
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

YVA (R–XBGA–N48) DIE–SIZE BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.
D. The package size (Dimension D and E) of a particular device is specified in the device Product Data Sheet version of this drawing, in case it cannot be found in the product data sheet please contact a local TI representative.
E. Reference Product Data Sheet for array population.
6 x 8 matrix pattern is shown for illustration only.
F. This package contains Pb–free balls.

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