

## REF20xx 低漂移、低功率、双路输出、 $V_{REF}$ 和 $V_{REF}/2$ 电压基准

### 1 特性

- 两个输出： $V_{REF}$  和  $V_{REF}/2$ ，便于在单电源系统中使用
- 优异的温度漂移性能：
  - $-40^{\circ}\text{C}$  至  $125^{\circ}\text{C}$  时为  $8\text{ ppm}/^{\circ}\text{C}$ （最大值）
- 高初始精度： $\pm 0.05\%$ （最大值）
- 温度范围内的  $V_{REF}$  和  $V_{BIAS}$  跟踪：
  - $-40^{\circ}\text{C}$  至  $85^{\circ}\text{C}$  时为  $6\text{ ppm}/^{\circ}\text{C}$ （最大值）
  - $-40^{\circ}\text{C}$  至  $125^{\circ}\text{C}$  时为  $7\text{ ppm}/^{\circ}\text{C}$ （最大值）
- 微型封装：SOT23-5
- 低压降电压：10mV
- 高输出电流： $\pm 20\text{mA}$
- 低静态电流： $360\mu\text{A}$
- 线路调节： $3\text{ ppm}/\text{V}$
- 负载调节： $8\text{ ppm}/\text{mA}$
- **Matte-Sn 版本 (REF2025AISDDCR) 在 Battelle Class III 和类似严苛环境中的抗腐蚀性得以改进**

### 2 应用

- 数字信号处理：
  - 电源逆变器
  - 电机控制
- 电流感测
- 工业过程控制
- 医疗设备
- 数据采集系统
- 单电源系统

### 3 说明

仅具有正向电源电压的应用通常需要一个在模数转换器 (ADC) 输入范围中间位置的附加稳定电压来偏置输入双极信号。REF20xx 提供了一个可供 ADC 使用的基准电压 ( $V_{REF}$ ) 和一个可用于偏置输入双极信号的高精度电压 ( $V_{BIAS}$ )。

REF20xx 在  $V_{REF}$  和  $V_{BIAS}$  输出端具有优异的温度漂移（最大  $8\text{ ppm}/^{\circ}\text{C}$ ）特性和初始精度 ( $0.05\%$ )，同时可保持静态工作电流低于  $430\mu\text{A}$ 。此外， $V_{REF}$  和  $V_{BIAS}$  输出端可在  $-40^{\circ}\text{C}$  至  $85^{\circ}\text{C}$  的温度范围内彼此跟踪，精度达  $6\text{ ppm}/^{\circ}\text{C}$ （最大值）。所有这些特性都可提高信号链的精度并节省电路板空间，相比分立式解决方案而言还能降低系统成本。仅  $10\text{mV}$  的超低压降允许器件在极低输入电压条件下工作，这一特性在电池供电系统中非常适用。

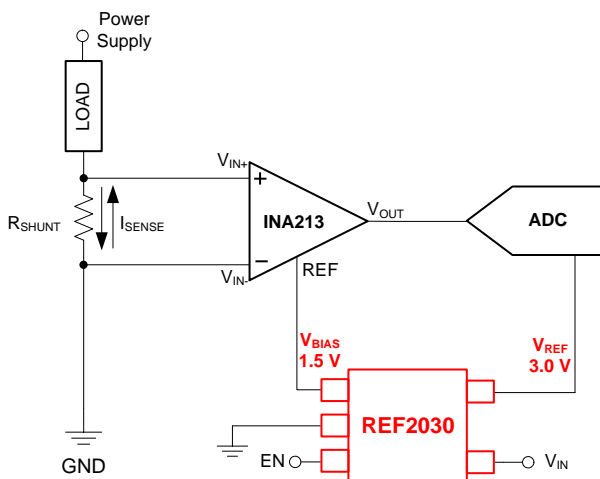
$V_{REF}$  和  $V_{BIAS}$  电压具有同样出色的技术规范，而且灌电流和拉电流能力同样强大。这些器件具有优异的长期稳定性和低噪声级别，是高精度工业应用。

器件信息(1)

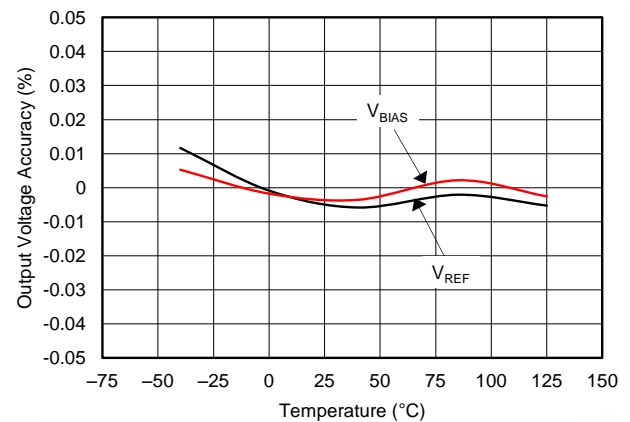
部件名称	封装	封装尺寸 (标称值)
REF20xx	小外形尺寸晶体管 (SOT) (5)	2.90mm × 1.60mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

应用示例



$V_{REF}$  和  $V_{BIAS}$  与温度间的关系



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## 4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

<b>Changes from Revision C (January 2017) to Revision D</b>	<b>Page</b>
• Changed application information to include corrosion resistance advantages. ....	<b>18</b>

<b>Changes from Revision B (July 2014) to Revision C</b>	<b>Page</b>
• Added I/O column to <i>Pin Functions</i> table .....	<b>3</b>
• Added <i>Storage temperature</i> parameter to <i>Absolute Maximum Ratings</i> table (moved from <i>ESD Ratings</i> table).....	<b>4</b>
• Changed <i>ESD Rating</i> table: changed title, updated table format .....	<b>4</b>

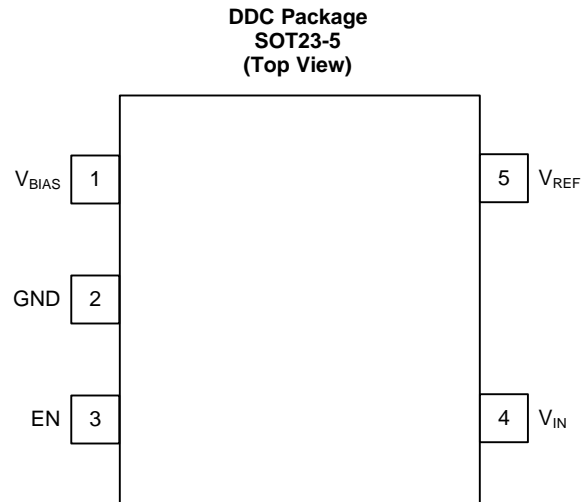
<b>Changes from Revision A (June 2014) to Revision B</b>	<b>Page</b>
• 器件状态从混合状态更改为生产数据 .....	<b>1</b>
• 删除了器件信息表中的脚注 2.....	<b>1</b>
• Deleted footnote from Device Comparison Table .....	<b>3</b>
• Added Thermal Information table .....	<b>4</b>

<b>Changes from Original (May 2014) to Revision A</b>	<b>Page</b>
• 更改了产品预览数据表 .....	<b>1</b>

## 5 Device Comparison Table

PRODUCT	$V_{REF}$	$V_{BIAS}$
REF2025	2.5 V	1.25 V
REF2030	3.0 V	1.5 V
REF2033	3.3 V	1.65 V
REF2041	4.096 V	2.048 V

## 6 Pin Configuration and Functions



### Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	$V_{BIAS}$	Output	Bias voltage output ( $V_{REF} / 2$ )
2	GND	—	Ground
3	EN	Input	Enable ( $EN \geq V_{IN} - 0.7\text{ V}$ , device enabled)
4	$V_{IN}$	Input	Input supply voltage
5	$V_{REF}$	Output	Reference voltage output ( $V_{REF}$ )

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Input voltage	V <sub>IN</sub>	-0.3	6	V
	EN	-0.3	V <sub>IN</sub> + 0.3	
Temperature	Operating	-55	150	°C
	Junction, T <sub>j</sub>		150	
	Storage, T <sub>stg</sub>	-65	170	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 7.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub> Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±4000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V <sub>IN</sub>	Supply input voltage range (I <sub>L</sub> = 0 mA, T <sub>A</sub> = 25°C)	V <sub>REF</sub> + 0.02 <sup>(1)</sup>		5.5	V

(1) See [Figure 28](#) in [Typical Characteristics](#) for minimum input voltage at different load currents and temperature

### 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		REF20xx	UNIT
		DDC (SOT23)	
		5 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	193.6	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	40.2	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	34.5	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	0.9	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	34.3	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 7.5 Electrical Characteristics

At  $T_A = 25^\circ\text{C}$ ,  $I_L = 0\text{ mA}$ , and  $V_{IN} = 5\text{ V}$ , unless otherwise noted. Both  $V_{REF}$  and  $V_{BIAS}$  have the same specifications.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>ACCURACY AND DRIFT</b>						
Output voltage accuracy			-0.05%		0.05%	
Output voltage temperature coefficient <sup>(1)</sup>		$-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$		$\pm 3$	$\pm 8$	ppm/ $^\circ\text{C}$
$V_{REF}$ and $V_{BIAS}$ tracking over temperature <sup>(2)</sup>		$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$		$\pm 1.5$	$\pm 6$	ppm/ $^\circ\text{C}$
		$-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$		$\pm 2$	$\pm 7$	
<b>LINE AND LOAD REGULATION</b>						
$\Delta V_{O(\Delta V_I)}$	Line regulation	$V_{REF} + 0.02\text{ V} \leq V_{IN} \leq 5.5\text{ V}$		3	35	ppm/V
$\Delta V_{O(\Delta I_L)}$	Load regulation	Sourcing $0\text{ mA} \leq I_L \leq 20\text{ mA}$ , $V_{REF} + 0.6\text{ V} \leq V_{IN} \leq 5.5\text{ V}$		8	20	ppm/mA
		Sinking $0\text{ mA} \leq I_L \leq -20\text{ mA}$ , $V_{REF} + 0.02\text{ V} \leq V_{IN} \leq 5.5\text{ V}$		8	20	
<b>POWER SUPPLY</b>						
$I_{CC}$	Supply current	Active mode $-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$		360	430	$\mu\text{A}$
					460	
Shutdown mode $-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$		3.3	5			
			9			
Enable voltage		Device in shutdown mode ( $EN = 0$ )	0		0.7	V
		Device in active mode ( $EN = 1$ )	$V_{IN} - 0.7$		$V_{IN}$	
Dropout voltage		$I_L = 20\text{ mA}$		10	20	mV
$I_{SC}$	Short-circuit current			50		mA
$t_{on}$	Turn-on time	0.1% settling, $C_L = 1\text{ }\mu\text{F}$		500		$\mu\text{s}$
<b>NOISE</b>						
Low-frequency noise <sup>(3)</sup>		$0.1\text{ Hz} \leq f \leq 10\text{ Hz}$		12		ppm <sub>PP</sub>
Output voltage noise density		$f = 100\text{ Hz}$		0.25		ppm/ $\sqrt{\text{Hz}}$
<b>CAPACITIVE LOAD</b>						
Stable output capacitor range			0		10	$\mu\text{F}$
<b>HYSTERESIS AND LONG TERM STABILITY</b>						
Long-term stability		0 to 1000 hours		60		ppm
Output voltage hysteresis <sup>(4)</sup>		$25^\circ\text{C}$ , $-40^\circ\text{C}$ , $125^\circ\text{C}$ , $25^\circ\text{C}$	Cycle 1	60		ppm
			Cycle 2	35		

(1) Temperature drift is specified according to the box method. See the [Feature Description](#) section for more details.

(2) The  $V_{REF}$  and  $V_{BIAS}$  tracking over temperature specification is explained in more detail in the [Feature Description](#) section.

(3) The peak-to-peak noise measurement procedure is explained in more detail in the [Noise Performance](#) section.

(4) The thermal hysteresis measurement procedure is explained in more detail in the [Thermal Hysteresis](#) section.

## 7.6 Typical Characteristics

At  $T_A = 25^\circ\text{C}$ ,  $I_L = 0\text{ mA}$ ,  $V_{IN} = 5\text{-V}$  power supply,  $C_L = 0\text{ }\mu\text{F}$ , and  $2.5\text{-V}$  output, unless otherwise noted.

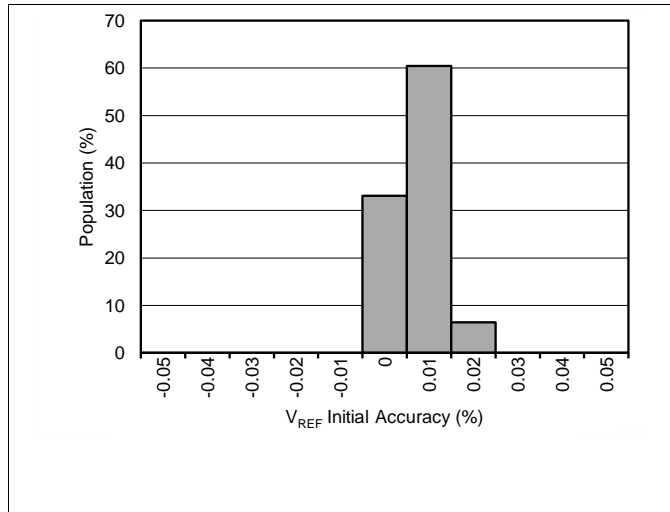


Figure 1. Initial Accuracy Distribution ( $V_{REF}$ )

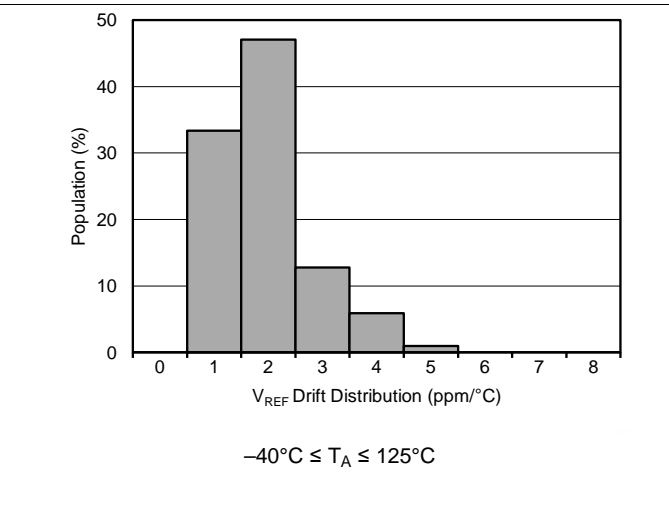


Figure 2. Drift Distribution ( $V_{REF}$ )

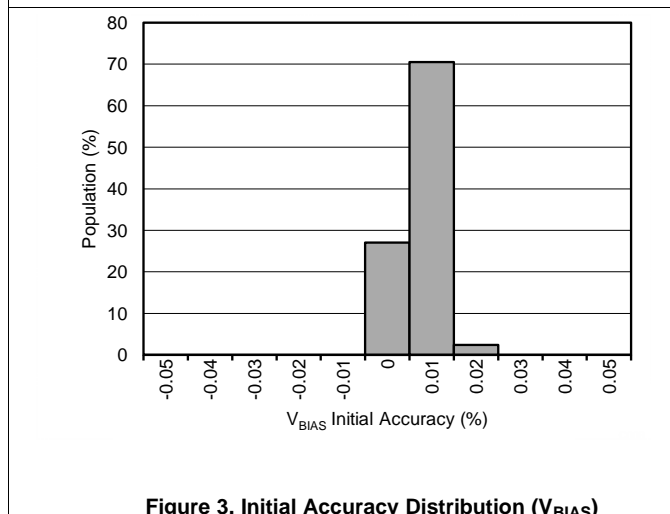


Figure 3. Initial Accuracy Distribution ( $V_{BIAS}$ )

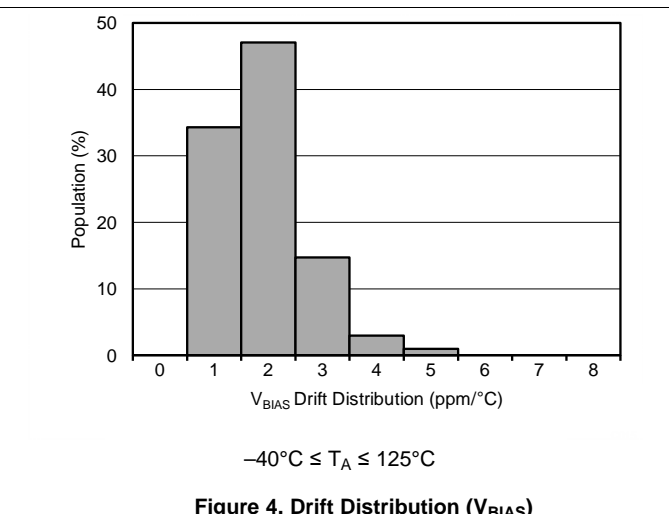


Figure 4. Drift Distribution ( $V_{BIAS}$ )

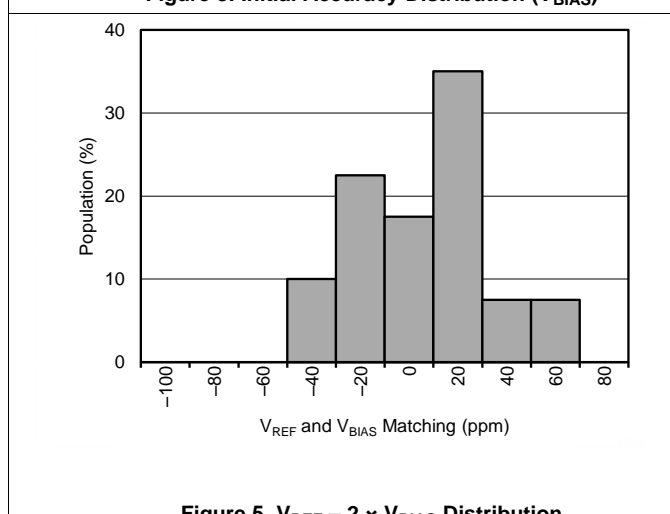


Figure 5.  $V_{REF} - 2 \times V_{BIAS}$  Distribution

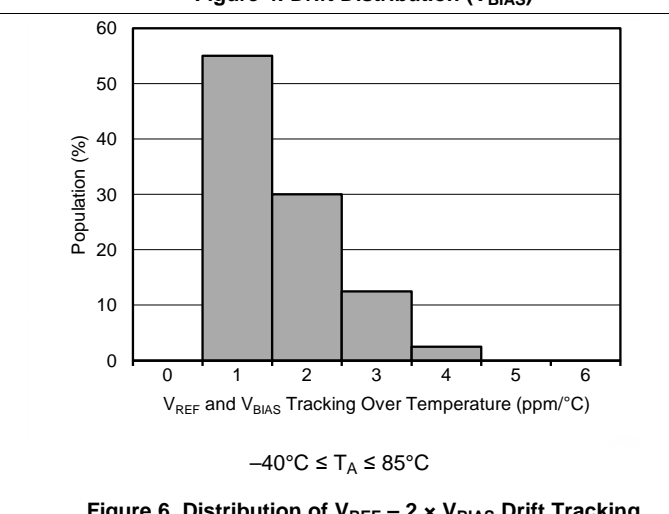
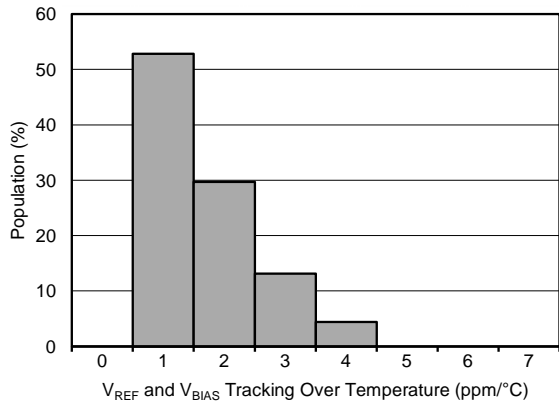


Figure 6. Distribution of  $V_{REF} - 2 \times V_{BIAS}$  Drift Tracking Over Temperature

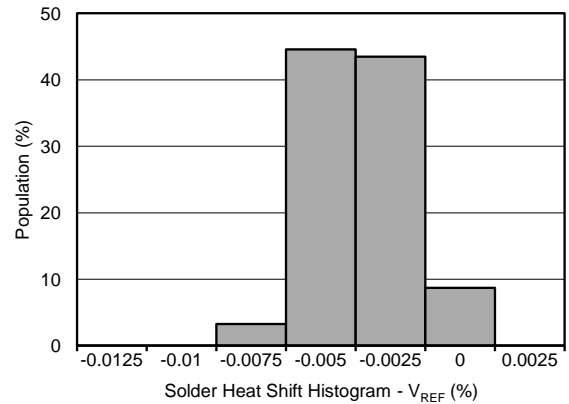
Typical Characteristics (continued)

At  $T_A = 25^\circ\text{C}$ ,  $I_L = 0\text{ mA}$ ,  $V_{IN} = 5\text{-V}$  power supply,  $C_L = 0\text{ }\mu\text{F}$ , and  $2.5\text{-V}$  output, unless otherwise noted.



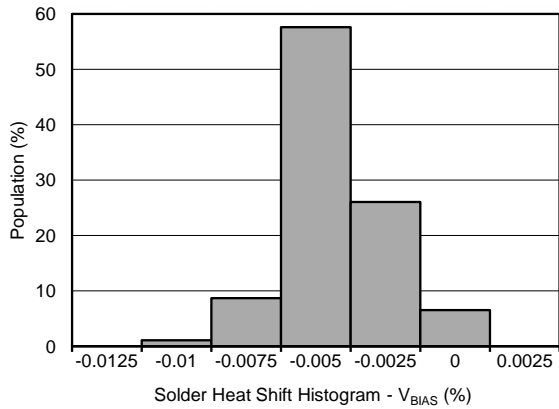
$-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$

Figure 7. Distribution of  $V_{REF} - 2 \times V_{BIAS}$  Drift Tracking Over Temperature



Refer to the [Solder Heat Shift](#) section for more information.

Figure 8. Solder Heat Shift Distribution ( $V_{REF}$ )



Refer to the [Solder Heat Shift](#) section for more information.

Figure 9. Solder Heat Shift Distribution ( $V_{BIAS}$ )

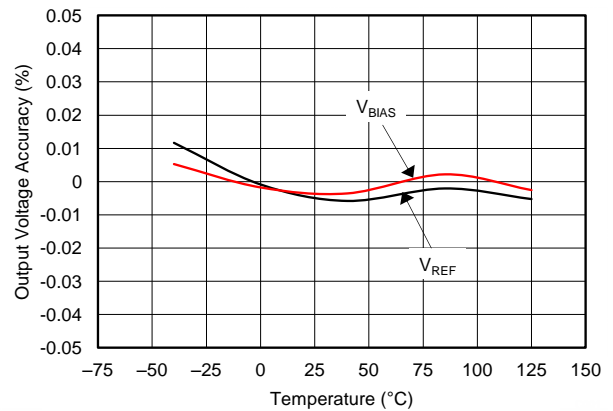


Figure 10. Output Voltage Accuracy ( $V_{REF}$ ) vs Temperature

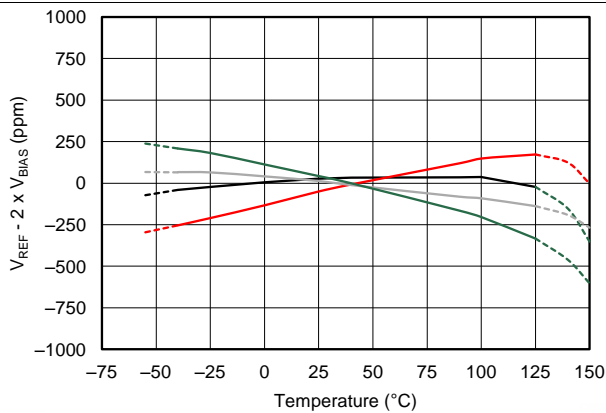


Figure 11.  $V_{REF} - 2 \times V_{BIAS}$  Tracking vs Temperature

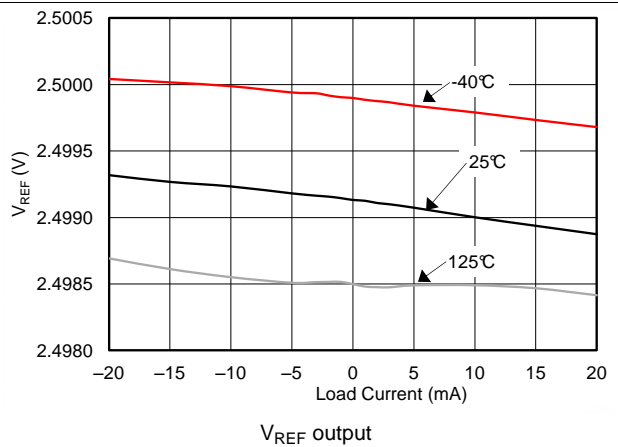


Figure 12. Output Voltage Change vs Load Current ( $V_{REF}$ )

### Typical Characteristics (continued)

At  $T_A = 25^\circ\text{C}$ ,  $I_L = 0\text{ mA}$ ,  $V_{IN} = 5\text{-V}$  power supply,  $C_L = 0\text{ }\mu\text{F}$ , and  $2.5\text{-V}$  output, unless otherwise noted.

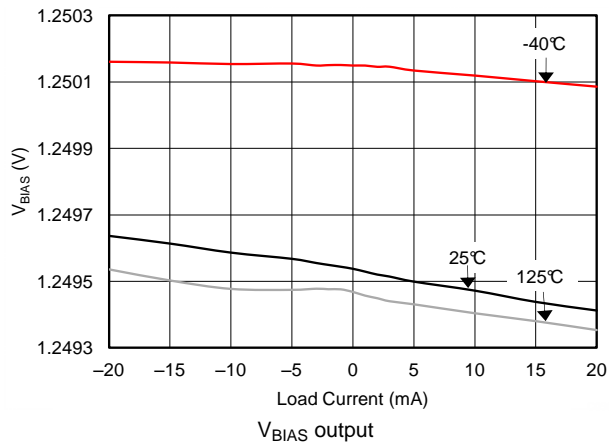


Figure 13. Output Voltage Change vs Load Current ( $V_{BIAS}$ )

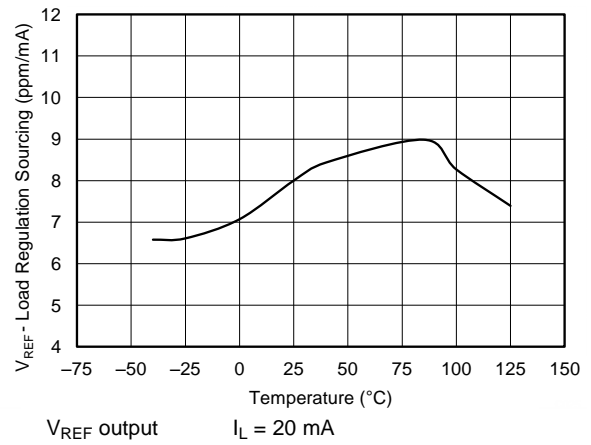


Figure 14. Load Regulation Sourcing vs Temperature ( $V_{REF}$ )

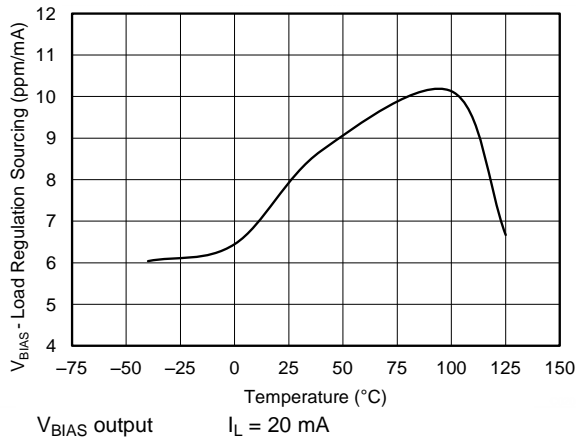


Figure 15. Load Regulation Sourcing vs Temperature ( $V_{BIAS}$ )

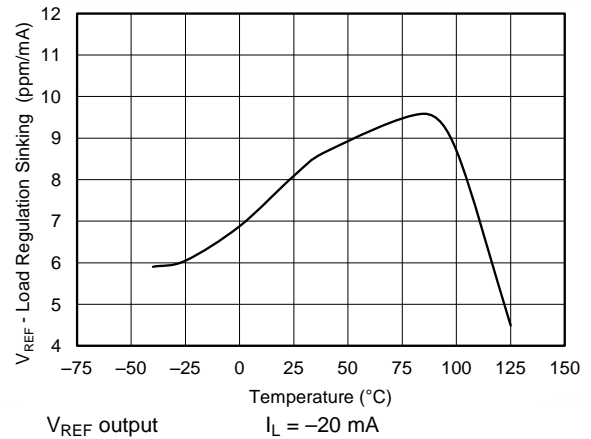


Figure 16. Load Regulation Sinking vs Temperature ( $V_{REF}$ )

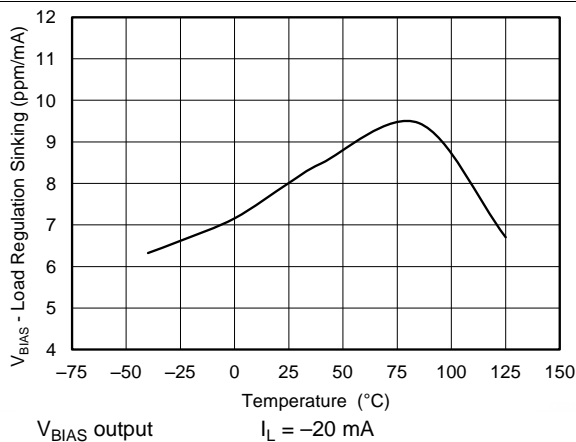


Figure 17. Load Regulation Sinking vs Temperature ( $V_{BIAS}$ )

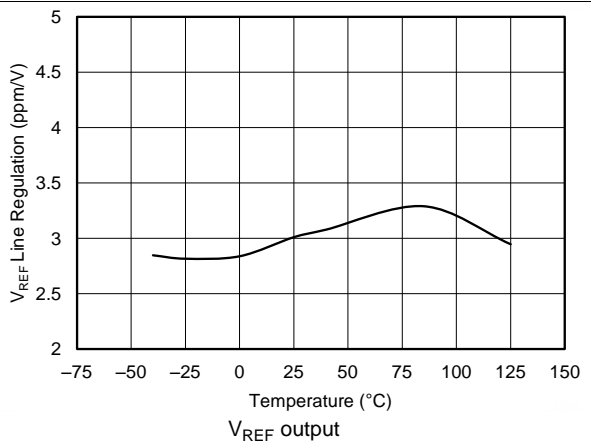


Figure 18. Line Regulation vs Temperature ( $V_{REF}$ )

Typical Characteristics (continued)

At  $T_A = 25^\circ\text{C}$ ,  $I_L = 0\text{ mA}$ ,  $V_{IN} = 5\text{-V}$  power supply,  $C_L = 0\text{ }\mu\text{F}$ , and  $2.5\text{-V}$  output, unless otherwise noted.

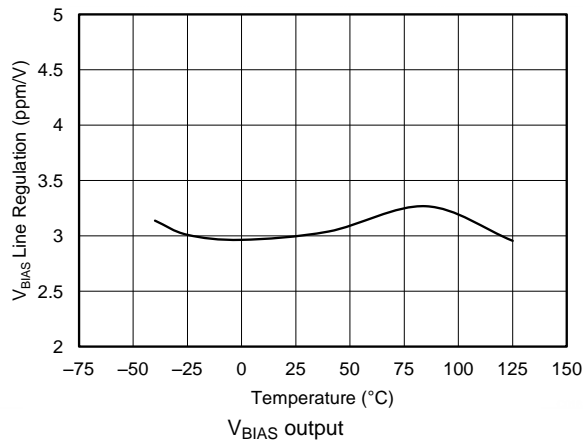


Figure 19. Line Regulation vs Temperature ( $V_{BIAS}$ )

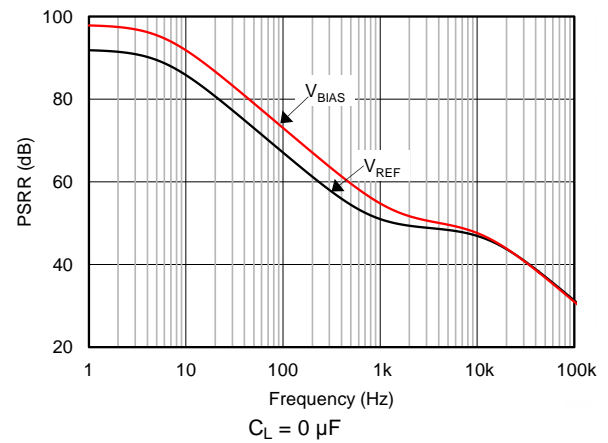


Figure 20. Power-Supply Rejection Ratio vs Frequency

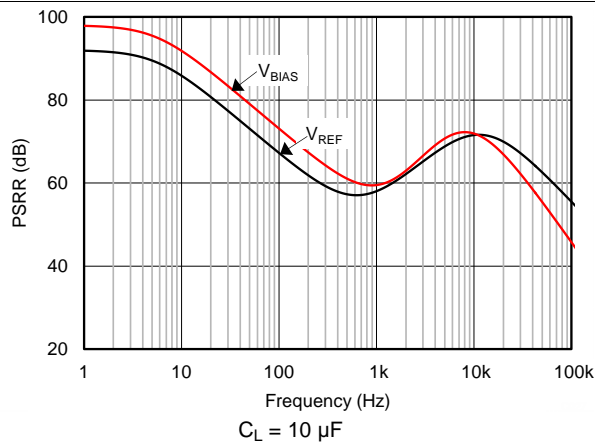


Figure 21. Power-Supply Rejection Ratio vs Frequency

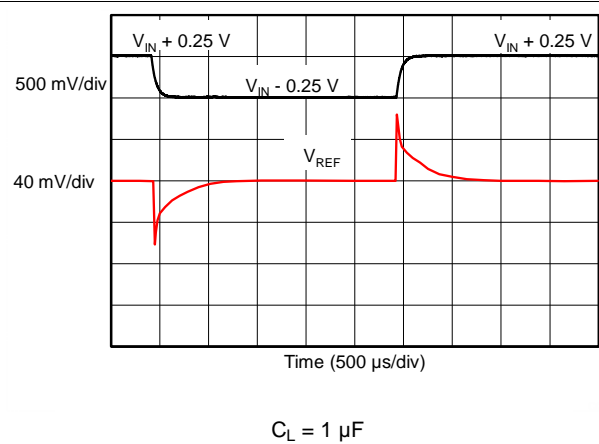


Figure 22. Line Transient Response

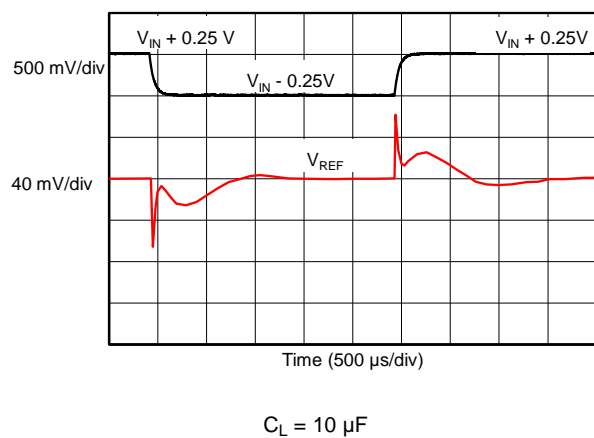


Figure 23. Line Transient Response

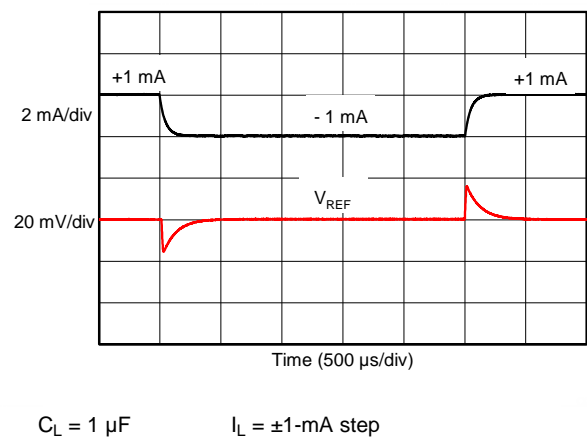
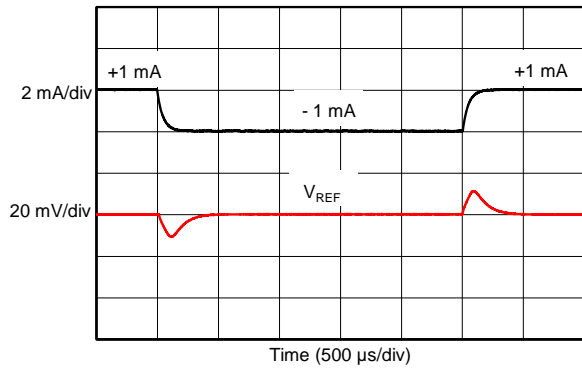


Figure 24. Load Transient Response

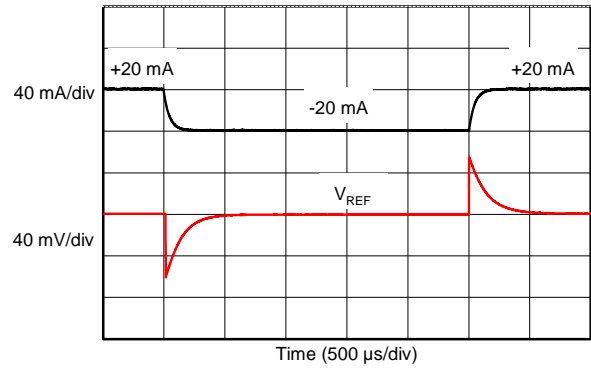
### Typical Characteristics (continued)

At  $T_A = 25^\circ\text{C}$ ,  $I_L = 0\text{ mA}$ ,  $V_{IN} = 5\text{-V}$  power supply,  $C_L = 0\text{ }\mu\text{F}$ , and  $2.5\text{-V}$  output, unless otherwise noted.



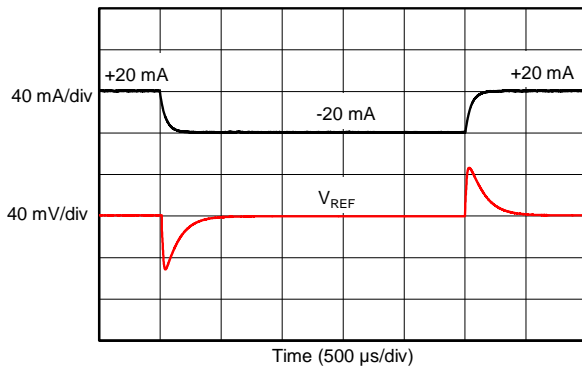
$C_L = 10\text{ }\mu\text{F}$       $I_L = \pm 1\text{-mA}$  step

**Figure 25. Load Transient Response**



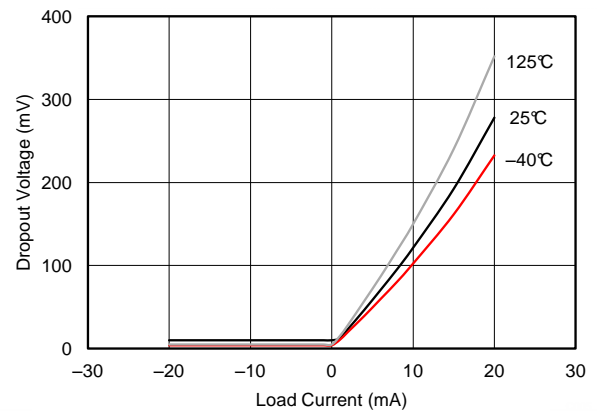
$C_L = 1\text{ }\mu\text{F}$       $I_L = \pm 20\text{-mA}$  step

**Figure 26. Load Transient Response**

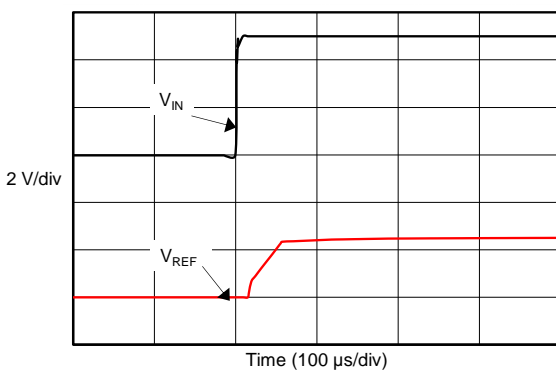


$C_L = 10\text{ }\mu\text{F}$       $I_L = \pm 20\text{-mA}$  step

**Figure 27. Load Transient Response**

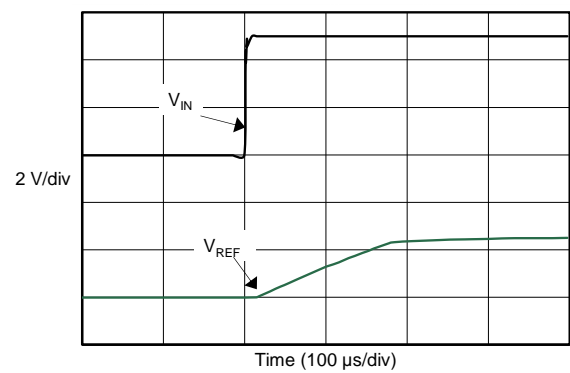


**Figure 28. Minimum Dropout Voltage vs Load Current**



$C_L = 1\text{ }\mu\text{F}$

**Figure 29. Turn-On Settling Time**



$C_L = 10\text{ }\mu\text{F}$

**Figure 30. Turn-On Settling Time**

### Typical Characteristics (continued)

At  $T_A = 25^\circ\text{C}$ ,  $I_L = 0\text{ mA}$ ,  $V_{IN} = 5\text{-V}$  power supply,  $C_L = 0\text{ }\mu\text{F}$ , and 2.5-V output, unless otherwise noted.

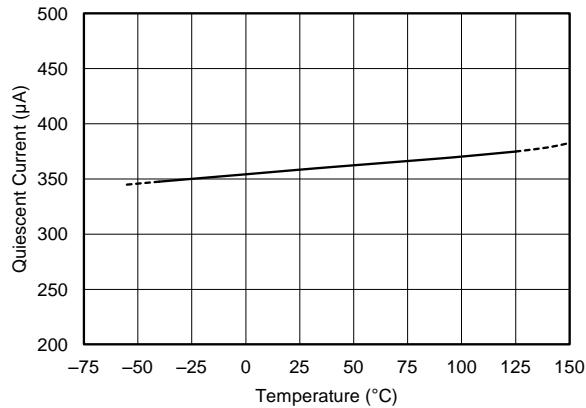


Figure 31. Quiescent Current vs Temperature

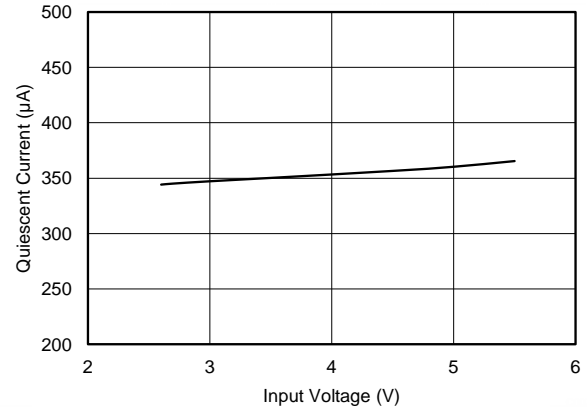
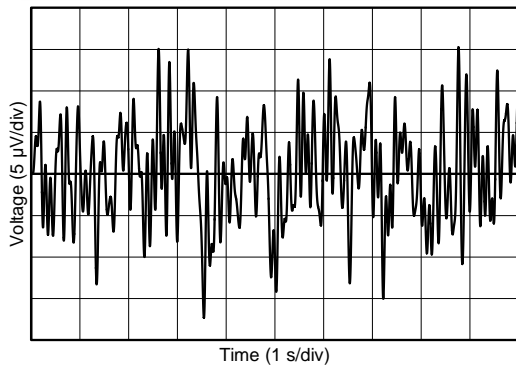
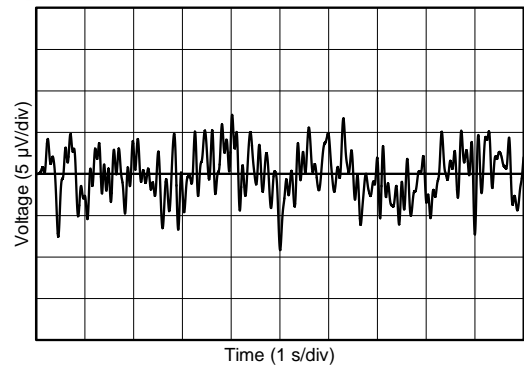


Figure 32. Quiescent Current vs Input Voltage



$V_{REF}$  output

Figure 33. 0.1-Hz to 10-Hz Noise ( $V_{REF}$ )



$V_{BIAS}$  output

Figure 34. 0.1-Hz to 10-Hz Noise ( $V_{BIAS}$ )

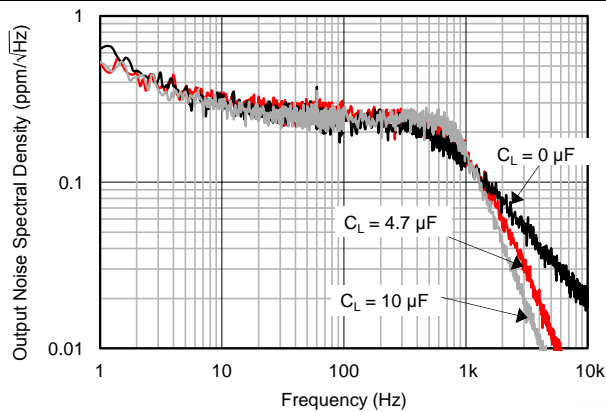


Figure 35. Output Voltage Noise Spectrum

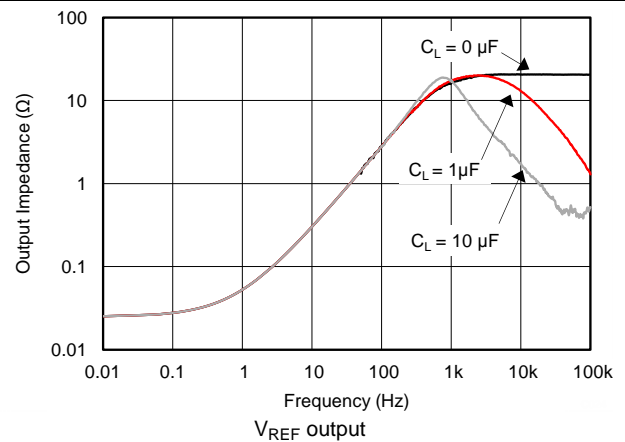
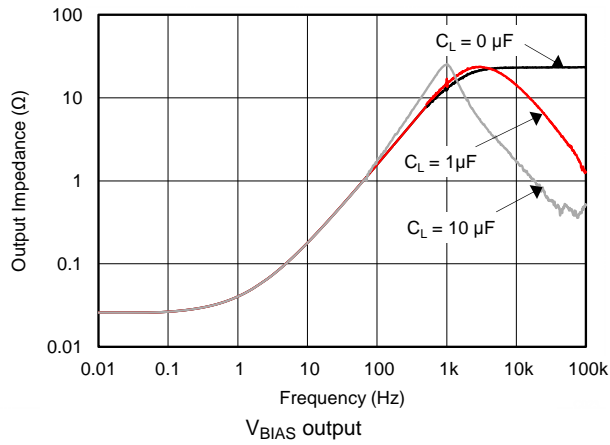


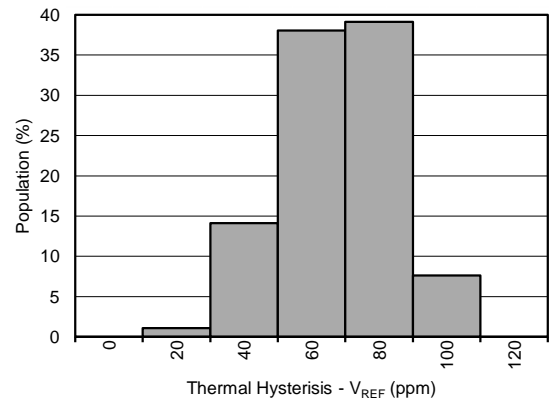
Figure 36. Output Impedance vs Frequency ( $V_{REF}$ )

**Typical Characteristics (continued)**

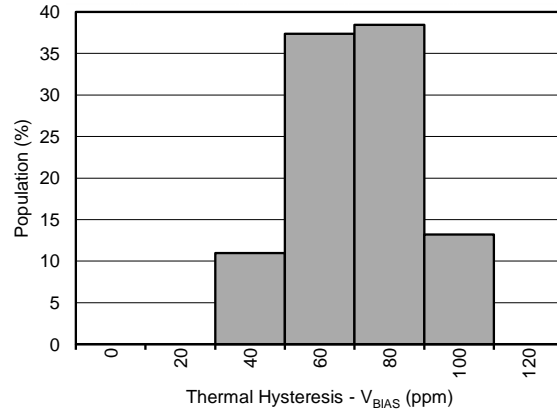
At  $T_A = 25^\circ\text{C}$ ,  $I_L = 0\text{ mA}$ ,  $V_{IN} = 5\text{-V}$  power supply,  $C_L = 0\ \mu\text{F}$ , and 2.5-V output, unless otherwise noted.



**Figure 37. Output Impedance vs Frequency ( $V_{BIAS}$ )**



**Figure 38. Thermal Hysteresis Distribution ( $V_{REF}$ )**



**Figure 39. Thermal Hysteresis Distribution ( $V_{BIAS}$ )**

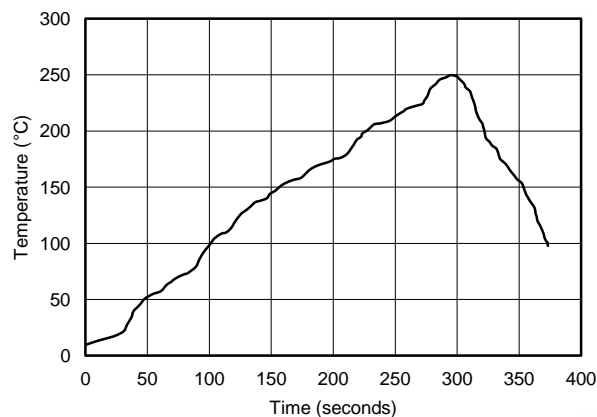
## 8 Parameter Measurement Information

### 8.1 Solder Heat Shift

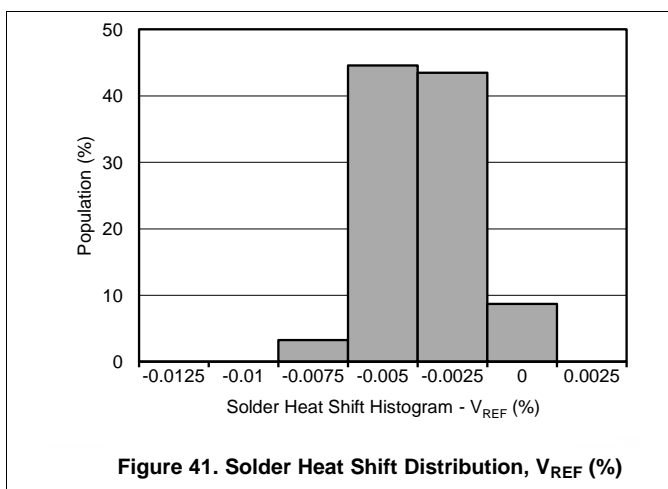
The materials used in the manufacture of the REF20xx have differing coefficients of thermal expansion, resulting in stress on the device die when the part is heated. Mechanical and thermal stress on the device die can cause the output voltages to shift, degrading the initial accuracy specifications of the product. Reflow soldering is a common cause of this error.

In order to illustrate this effect, a total of 92 devices were soldered on four printed circuit boards [23 devices on each printed circuit board (PCB)] using lead-free solder paste and the paste manufacturer suggested reflow profile. The reflow profile is as shown in Figure 40. The printed circuit board is comprised of FR4 material. The board thickness is 1.57 mm and the area is 171.54 mm × 165.1 mm.

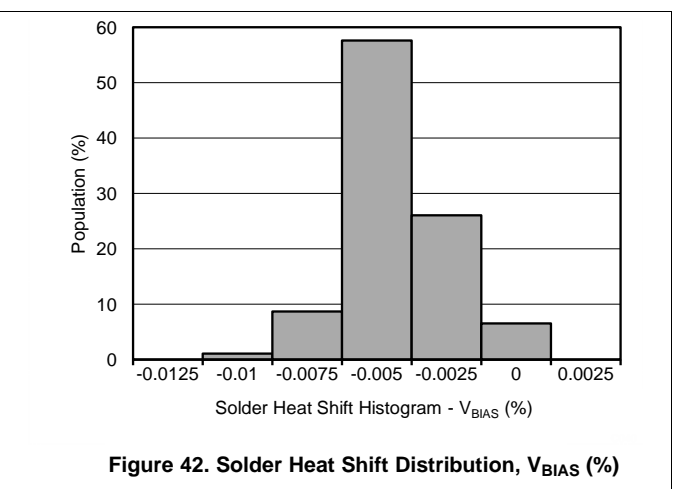
The reference and bias output voltages are measured before and after the reflow process; the typical shift is displayed in Figure 41 and Figure 42. Although all tested units exhibit very low shifts (< 0.01%), higher shifts are also possible depending on the size, thickness, and material of the printed circuit board. An important note is that the histograms display the typical shift for exposure to a single reflow profile. Exposure to multiple reflows, as is common on PCBs with surface-mount components on both sides, causes additional shifts in the output bias voltage. If the PCB is exposed to multiple reflows, the device should be soldered in the second pass to minimize its exposure to thermal stress.



**Figure 40. Reflow Profile**



**Figure 41. Solder Heat Shift Distribution, V<sub>REF</sub> (%)**



**Figure 42. Solder Heat Shift Distribution, V<sub>BIAS</sub> (%)**

## 8.2 Thermal Hysteresis

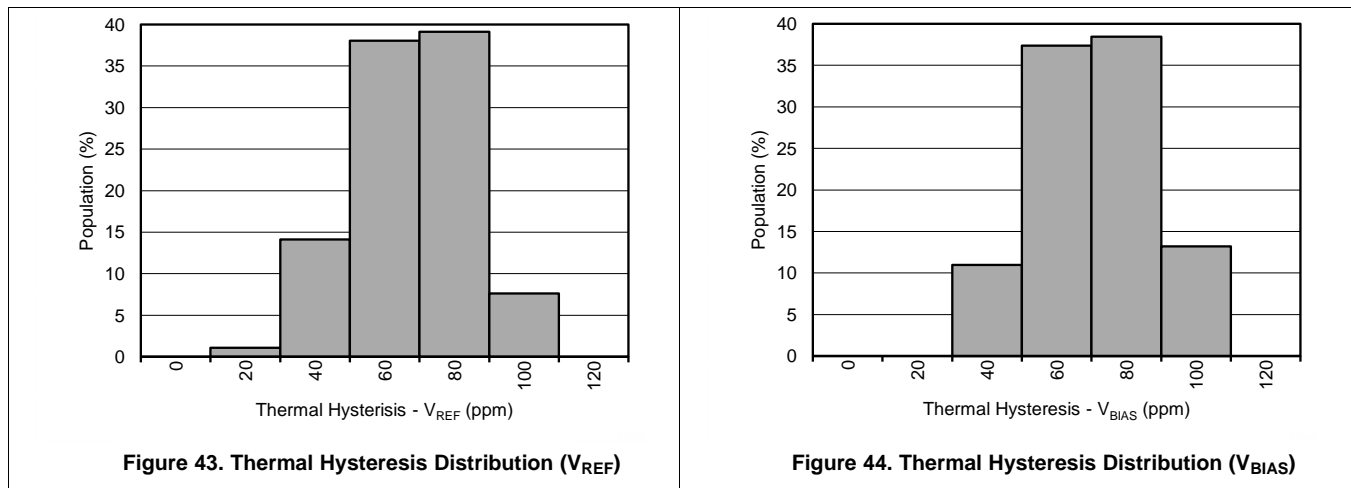
Thermal hysteresis is measured with the REF20xx soldered to a PCB, similar to a real-world application. Thermal hysteresis for the device is defined as the change in output voltage after operating the device at 25°C, cycling the device through the specified temperature range, and returning to 25°C. Hysteresis can be expressed by [Equation 1](#):

$$V_{\text{HYST}} = \left( \frac{|V_{\text{PRE}} - V_{\text{POST}}|}{V_{\text{NOM}}} \right) \cdot 10^6 \text{ (ppm)}$$

where

- $V_{\text{HYST}}$  = thermal hysteresis (in units of ppm),
- $V_{\text{NOM}}$  = the specified output voltage,
- $V_{\text{PRE}}$  = output voltage measured at 25°C pre-temperature cycling, and
- $V_{\text{POST}}$  = output voltage measured after the device has cycled from 25°C through the specified temperature range of –40°C to 125°C and returns to 25°C. (1)

Typical thermal hysteresis distribution is as shown in [Figure 43](#) and [Figure 44](#).



### 8.3 Noise Performance

Typical 0.1-Hz to 10-Hz voltage noise can be seen in [Figure 45](#) and [Figure 46](#). Device noise increases with output voltage and operating temperature. Additional filtering can be used to improve output noise levels, although care should be taken to ensure the output impedance does not degrade ac performance. Peak-to-peak noise measurement setup is shown in [Figure 47](#).

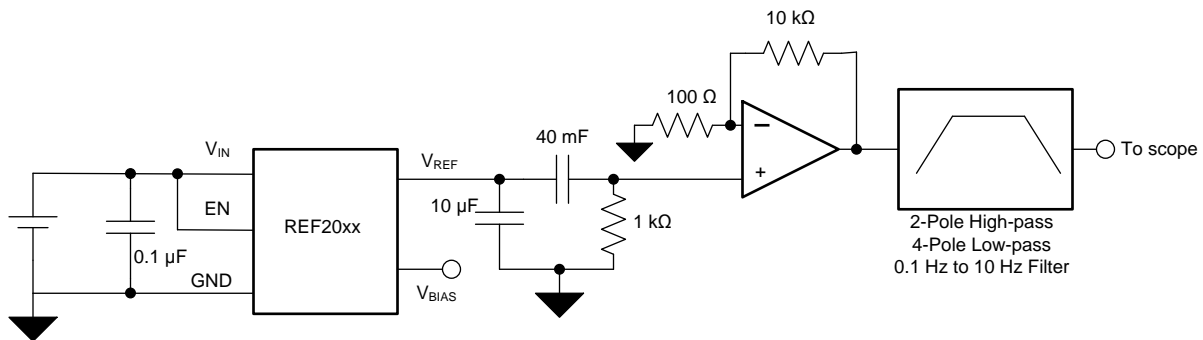
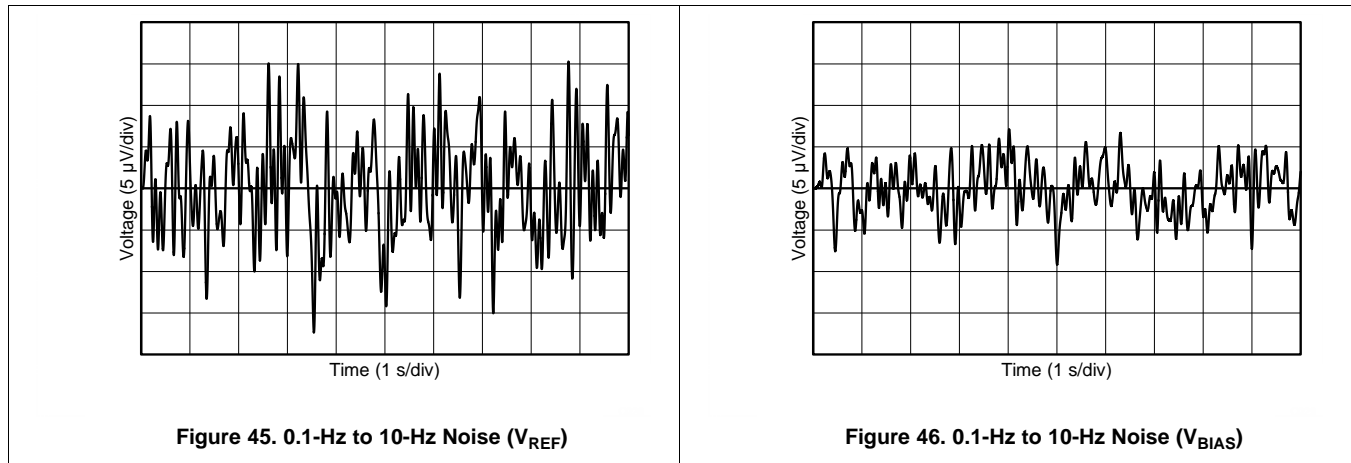


Figure 47. 0.1-Hz to 10-Hz Noise Measurement Setup

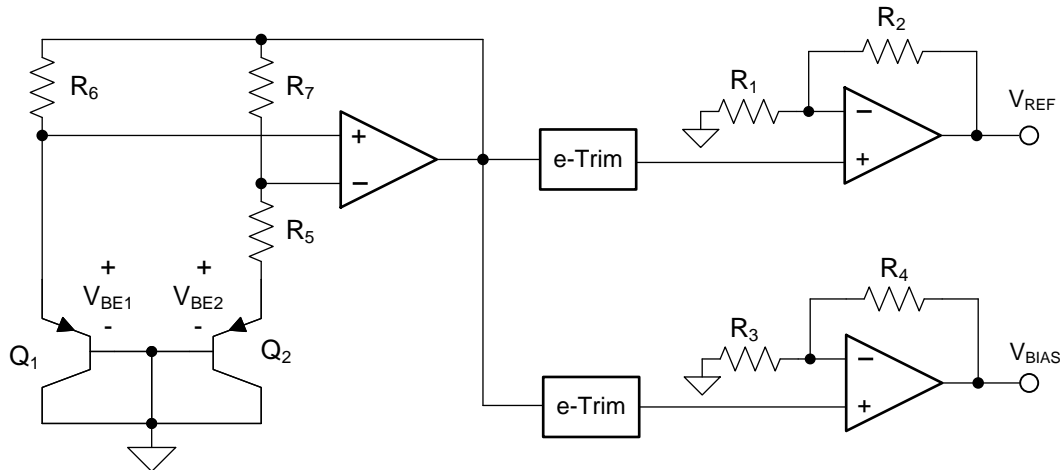
## 9 Detailed Description

### 9.1 Overview

The REF20xx are a family of dual-output,  $V_{REF}$  and  $V_{BIAS}$  ( $V_{REF} / 2$ ) band-gap voltage references. The [Functional Block Diagram](#) section provides a block diagram of the basic band-gap topology and the two buffers used to derive the  $V_{REF}$  and  $V_{BIAS}$  outputs. Transistors  $Q_1$  and  $Q_2$  are biased such that the current density of  $Q_1$  is greater than that of  $Q_2$ . The difference of the two base emitter voltages ( $V_{BE1} - V_{BE2}$ ) has a positive temperature coefficient and is forced across resistor  $R_5$ . The voltage is amplified and added to the base emitter voltage of  $Q_2$ , which has a negative temperature coefficient. The resulting band-gap output voltage is almost independent of temperature. Two independent buffers are used to generate  $V_{REF}$  and  $V_{BIAS}$  from the band-gap voltage. The resistors  $R_1$ ,  $R_2$  and  $R_3$ ,  $R_4$  are sized such that  $V_{BIAS} = V_{REF} / 2$ .

e-Trim™ is a method of package-level trim for the initial accuracy and temperature coefficient of  $V_{REF}$  and  $V_{BIAS}$ , implemented during the final steps of manufacturing after the plastic molding process. This method minimizes the influence of inherent transistor mismatch, as well as errors induced during package molding. e-Trim is implemented in the REF20xx to minimize the temperature drift and maximize the initial accuracy of both the  $V_{REF}$  and  $V_{BIAS}$  outputs.

### 9.2 Functional Block Diagram



### 9.3 Feature Description

#### 9.3.1 $V_{REF}$ and $V_{BIAS}$ Tracking

Most single-supply systems require an additional stable voltage in the middle of the analog-to-digital converter (ADC) input range to bias input bipolar signals. The  $V_{REF}$  and  $V_{BIAS}$  outputs of the REF20xx are generated from the same band-gap voltage as shown in the [Functional Block Diagram](#) section. Hence, both outputs track each other over the full temperature range of  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  with an accuracy of 7 ppm/ $^{\circ}\text{C}$  (max). The tracking accuracy increases to 6 ppm/ $^{\circ}\text{C}$  (max) when the temperature range is limited to  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ . The tracking error is calculated using the box method, as described by [Equation 2](#):

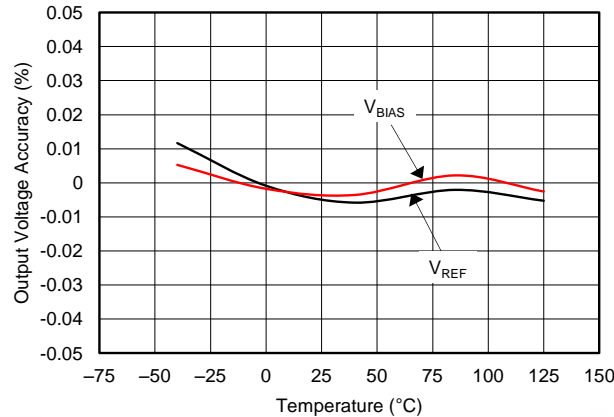
$$\text{Tracking Error} = \left( \frac{V_{\text{DIFF(MAX)}} - V_{\text{DIFF(MIN)}}}{V_{\text{REF}} \cdot \text{Temperature Range}} \right) \cdot 10^6 \quad (\text{ppm})$$

where

$$\bullet \quad V_{\text{DIFF}} = V_{\text{REF}} - 2 \cdot V_{\text{BIAS}} \quad (2)$$

## Feature Description (continued)

The tracking accuracy is as shown in [Figure 48](#).



**Figure 48. V<sub>REF</sub> and V<sub>BIAS</sub> Tracking vs Temperature**

### 9.3.2 Low Temperature Drift

The REF20xx is designed for minimal drift error, which is defined as the change in output voltage over temperature. The drift is calculated using the box method, as described by [Equation 3](#):

$$\text{Drift} = \left( \frac{V_{\text{REF(MAX)}} - V_{\text{REF(MIN)}}}{V_{\text{REF}} \cdot \text{Temperature Range}} \right) \cdot 10^6 \quad (\text{ppm}) \quad (3)$$

### 9.3.3 Load Current

The REF20xx family is specified to deliver a current load of  $\pm 20$  mA per output. Both the V<sub>REF</sub> and V<sub>BIAS</sub> outputs of the device are protected from short circuits by limiting the output short-circuit current to 50 mA. The device temperature increases according to [Equation 4](#):

$$T_J = T_A + P_D \cdot R_{\theta JA}$$

where

- T<sub>J</sub> = junction temperature (°C),
  - T<sub>A</sub> = ambient temperature (°C),
  - P<sub>D</sub> = power dissipated (W), and
  - R<sub>θJA</sub> = junction-to-ambient thermal resistance (°C/W)
- (4)

The REF20xx maximum junction temperature must not exceed the absolute maximum rating of 150°C.

## 9.4 Device Functional Modes

When the EN pin of the REF20xx is pulled high, the device is in active mode. The device should be in active mode for normal operation. The REF20xx can be placed in a low-power mode by pulling the ENABLE pin low. When in shutdown mode, the output of the device becomes high impedance and the quiescent current of the device reduces to 5 μA in shutdown mode. See the [Electrical Characteristics](#) for logic high and logic low voltage levels.

## 10 Applications and Implementation

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### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

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### 10.1 Application Information

The low-drift, bidirectional, single-supply, low-side, current-sensing solution, described in this section, can accurately detect load currents from  $-2.5\text{ A}$  to  $2.5\text{ A}$ . The linear range of the output is from  $250\text{ mV}$  to  $2.75\text{ V}$ . Positive current is represented by output voltages from  $1.5\text{ V}$  to  $2.75\text{ V}$ , whereas negative current is represented by output voltages from  $250\text{ mV}$  to  $1.5\text{ V}$ . The difference amplifier is the [INA213](#) current-shunt monitor, whose supply and reference voltages are supplied by the low-drift REF2030.

Industrial applications with electronics in corrosive environments are susceptible to corrosive damage due to the exposure to heat, moisture, and corrosive gases. The combination of the following conditions in a given system lead to higher risk of corrosive damage:

1. Ventilated enclosures exposing underlying PCB.
2. PCBs not conformally coated.
3. Exposed-lead components with plating susceptible to corrosion.
4. Changes in plating techniques for RoHS compliance (e.g. removal of Pb (lead) and certain types of plating).

To improve resistance to corrosion in harsh environments, the REF2025AISDDCR uses Matte-Sn plating with improved assembly process to reduce exposed Cu, leading to improved corrosion resistance in the Battelle Class III and similar harsh environments. The "S" in the part number identifies this special plating option. REF2025 versions that do not have the "S" will continue to be available in industry standard NiPdAu processing technique.

## 10.2 Typical Application

### 10.2.1 Low-Side, Current-Sensing Application

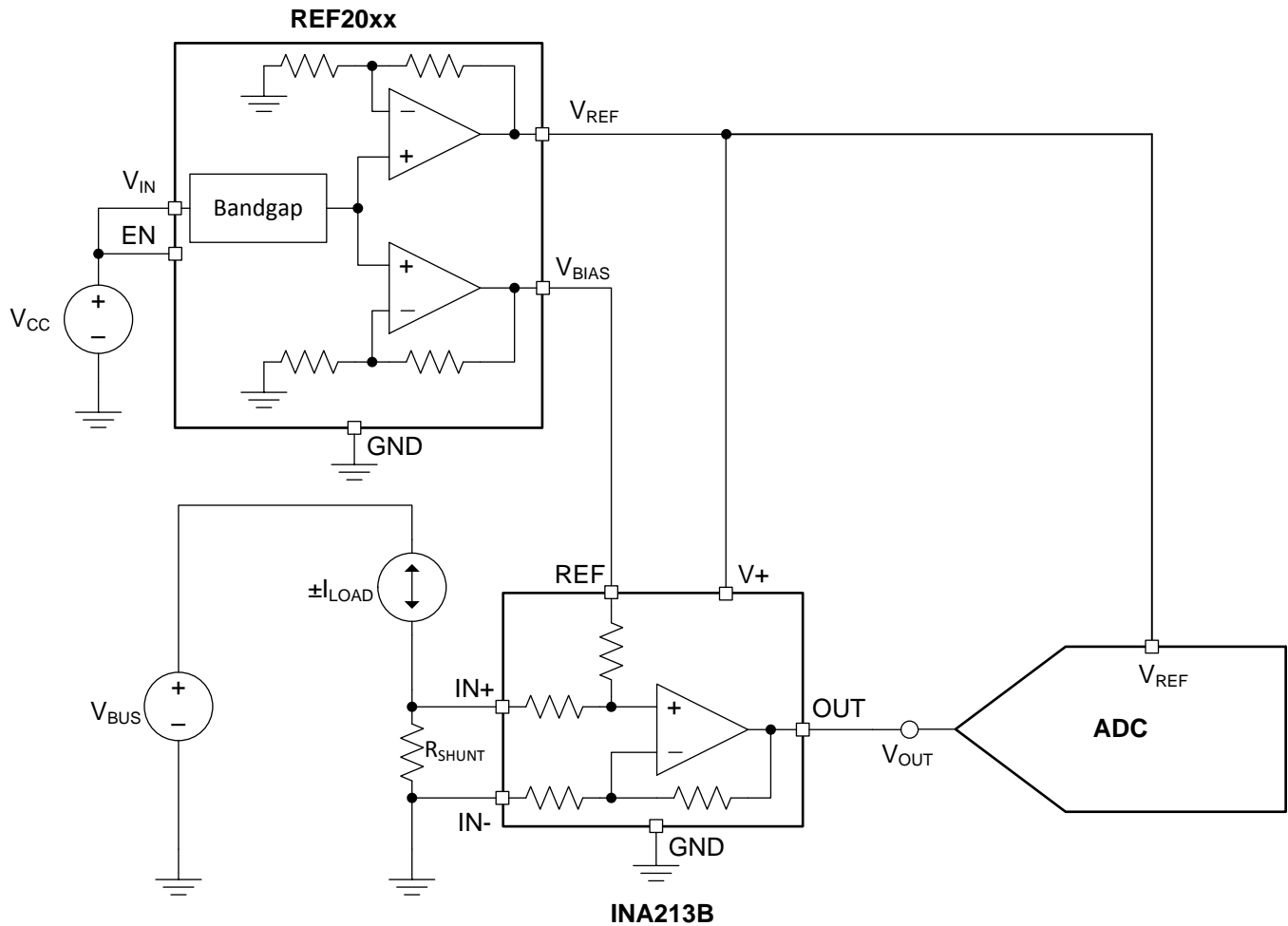


Figure 49. Low-Side, Current-Sensing Application

## Typical Application (continued)

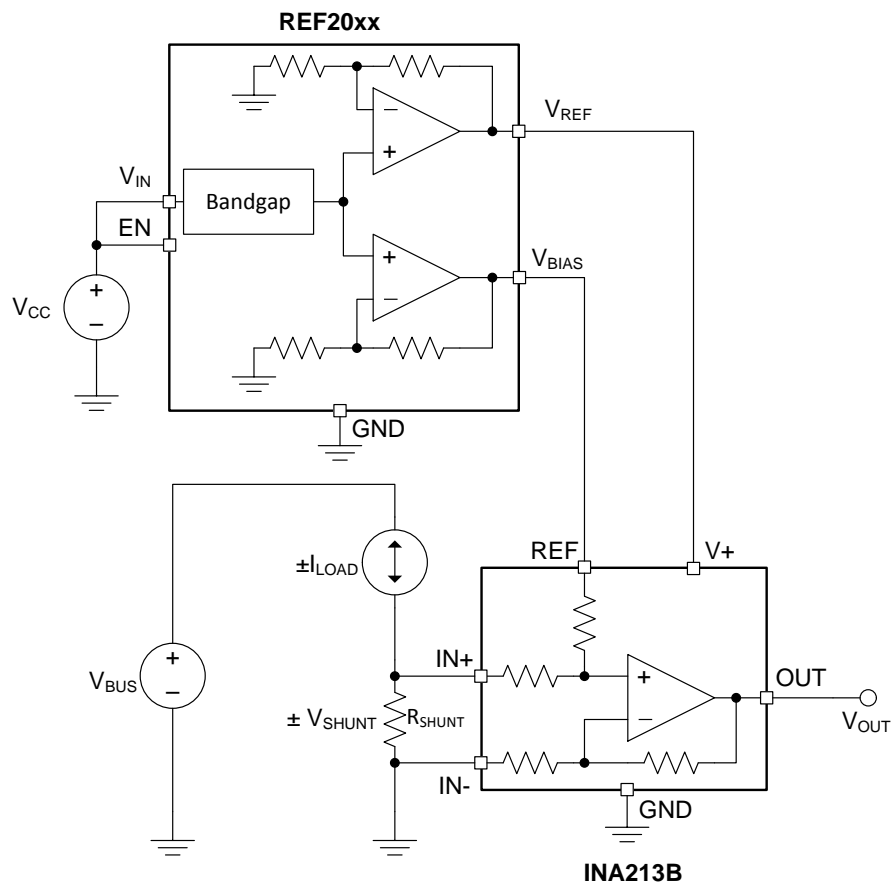
### 10.2.1.1 Design Requirements

The design requirements are as follows:

1. Supply voltage: 5.0 V
2. Load current:  $\pm 2.5$  A
3. Output: 250 mV to 2.75 V
4. Maximum shunt voltage:  $\pm 25$  mV

### 10.2.1.2 Detailed Design Procedure

Low-side current sensing is desirable because the common-mode voltage is near ground. Therefore, the current-sensing solution is independent of the bus voltage,  $V_{BUS}$ . When sensing bidirectional currents, use a differential amplifier with a reference pin. This procedure allows for the differentiation between positive and negative currents by biasing the output stage such that it can respond to negative input voltages. There are a variety of methods for supplying power ( $V+$ ) and the reference voltage ( $V_{REF}$ , or  $V_{BIAS}$ ) to the differential amplifier. For a low-drift solution, use a monolithic reference that supplies both power and the reference voltage. Figure 50 shows the general circuit topology for a low-drift, low-side, bidirectional, current-sensing solution. This topology is particularly useful when interfacing with an ADC; see Figure 49. Not only do  $V_{REF}$  and  $V_{BIAS}$  track over temperature, but their matching is much better than alternate topologies. For a more detailed version of the design procedure, refer to TIDU357.



**Figure 50. Low-Drift, Low-side, Bidirectional, Current-Sensing Circuit Topology**

The transfer function for the circuit given in Figure 50 is as shown in Equation 5:

$$\begin{aligned}
 V_{OUT} &= G \cdot (\pm V_{SHUNT}) + V_{BIAS} \\
 &= G \cdot (\pm I_{LOAD} \cdot R_{SHUNT}) + V_{BIAS}
 \end{aligned}
 \tag{5}$$

## Typical Application (continued)

### 10.2.1.2.1 Shunt Resistor

As illustrated in [Figure 50](#), the value of  $V_{SHUNT}$  is the ground potential for the system load. If the value of  $V_{SHUNT}$  is too large, issues may arise when interfacing with systems whose ground potential is actually 0 V. Also, a value of  $V_{SHUNT}$  that is too negative may violate the input common-mode voltage of the differential amplifier in addition to potential interfacing issues. Therefore, limiting the voltage across the shunt resistor is important. [Equation 6](#) can be used to calculate the maximum value of  $R_{SHUNT}$ .

$$R_{SHUNT(max)} = \frac{V_{SHUNT(max)}}{I_{LOAD(max)}} \quad (6)$$

Given that the maximum shunt voltage is  $\pm 25$  mV and the load current range is  $\pm 2.5$  A, the maximum shunt resistance is calculated as shown in [Equation 7](#).

$$R_{SHUNT(max)} = \frac{V_{SHUNT(max)}}{I_{LOAD(max)}} = \frac{25mV}{2.5A} = 10m\Omega \quad (7)$$

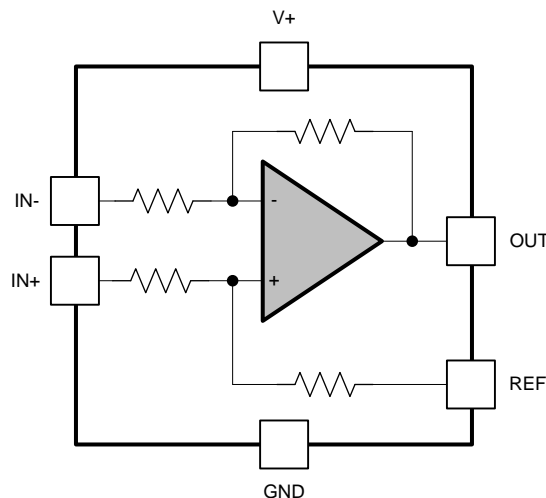
To minimize errors over temperature, select a low-drift shunt resistor. To minimize offset error, select a shunt resistor with the lowest tolerance. For this design, the Y14870R01000B9W resistor is used.

### 10.2.1.2.2 Differential Amplifier

The differential amplifier used for this design should have the following features:

1. Single-supply (3 V),
2. Reference voltage input,
3. Low initial input offset voltage ( $V_{OS}$ ),
4. Low-drift,
5. Fixed gain, and
6. Low-side sensing (input common-mode range below ground).

For this design, a current-shunt monitor (INA213) is used. The INA21x family topology is shown in [Figure 51](#). The INA213B specifications can be found in the [INA213 product data sheet](#).



Copyright © 2017, Texas Instruments Incorporated

**Figure 51. INA21x Current-Shunt Monitor Topology**

## Typical Application (continued)

The INA213B is an excellent choice for this application because all the required features are included. In general, instrumentation amplifiers (INAs) do not have the input common-mode swing to ground that is essential for this application. In addition, INAs require external resistors to set their gain, which is not desirable for low-drift applications. Difference amplifiers typically have larger input bias currents, which reduce solution accuracy at small load currents. Difference amplifiers typically have a gain of 1 V/V. When the gain is adjustable, these amplifiers use external resistors that are not conducive to low-drift applications.

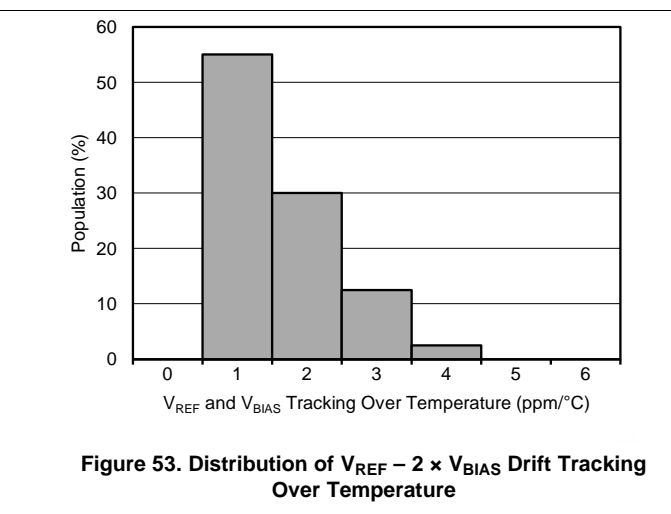
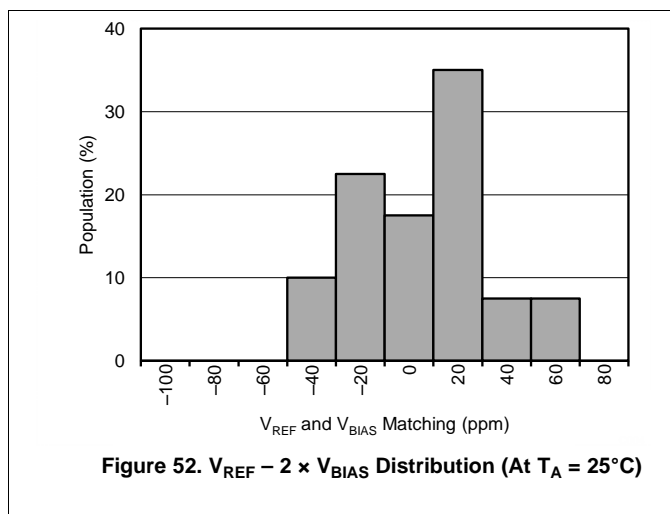
### 10.2.1.2.3 Voltage Reference

The voltage reference for this application should have the following features:

1. Dual output (3.0 V and 1.5 V),
2. Low drift, and
3. Low tracking errors between the two outputs.

For this design, the REF2030 is used. The REF20xx topology is as shown in the [Functional Block Diagram](#) section.

The REF2030 is an excellent choice for this application because of its dual output. The temperature drift of 8 ppm/°C and initial accuracy of 0.05% make the errors resulting from the voltage reference minimal in this application. In addition, there is minimal mismatch between the two outputs and both outputs track very well across temperature, as shown in [Figure 52](#) and [Figure 53](#).



### 10.2.1.2.4 Results

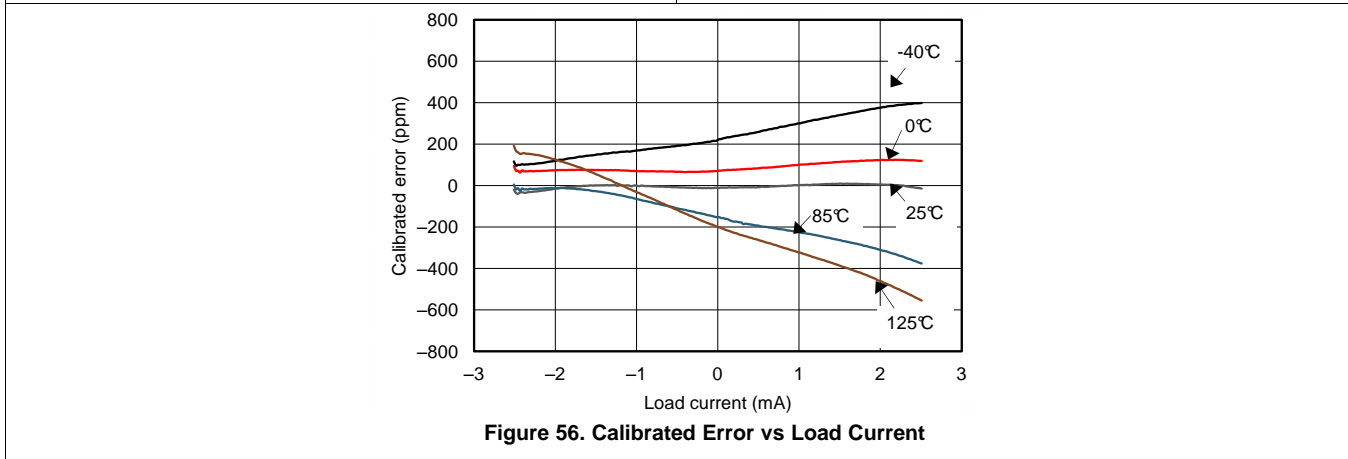
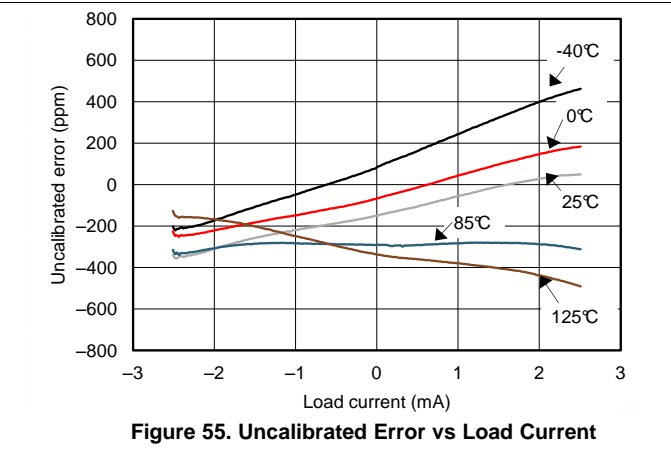
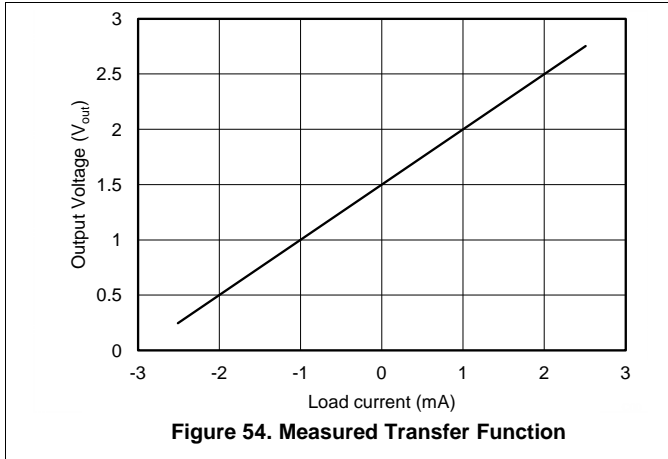
[Table 1](#) summarizes the measured results.

**Table 1. Measured Results**

ERROR	UNCALIBRATED (%)	CALIBRATED (%)
Error across the full load current range (25°C)	±0.0355	±0.004
Error across the full load current range (-40°C to 125°C)	±0.0522	±0.0606

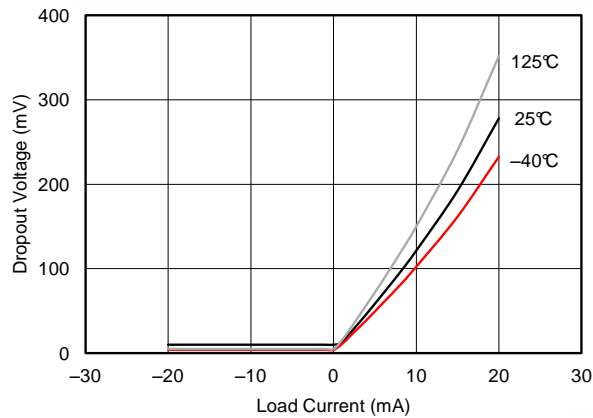
**10.2.1.3 Application Curves**

Performing a two-point calibration at 25°C removes the errors associated with offset voltage, gain error, and so forth. [Figure 54](#) to [Figure 56](#) show the measured error at different conditions. For a more detailed description on measurement procedure, calibration, and calculations, please refer to [TIDU357](#).



## 11 Power-Supply Recommendations

The REF20xx family of references feature an extremely low-dropout voltage. These references can be operated with a supply of only 20 mV above the output voltage. For loaded reference conditions, a typical dropout voltage versus load is shown in [Figure 57](#). A supply bypass capacitor ranging between 0.1  $\mu\text{F}$  to 10  $\mu\text{F}$  is recommended.



**Figure 57. Dropout Voltage vs Load Current**

## 12 Layout

### 12.1 Layout Guidelines

Figure 58 shows an example of a PCB layout for a data acquisition system using the REF2030. Some key considerations are:

- Connect low-ESR, 0.1- $\mu$ F ceramic bypass capacitors at  $V_{IN}$ ,  $V_{REF}$ , and  $V_{BIAS}$  of the REF2030.
- Decouple other active devices in the system per the device specifications.
- Using a solid ground plane helps distribute heat and reduces electromagnetic interference (EMI) noise pickup.
- Place the external components as close to the device as possible. This configuration prevents parasitic errors (such as the Seebeck effect) from occurring.
- Minimize trace length between the reference and bias connections to the INA and ADC to reduce noise pickup.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when absolutely necessary.

### 12.2 Layout Example

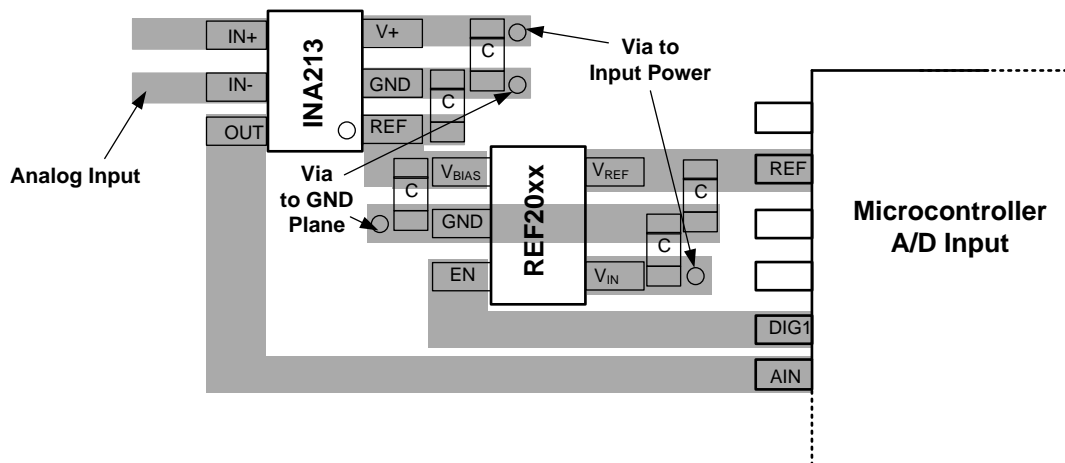


Figure 58. Layout Example

## 13 器件和文档支持

### 13.1 文档支持

#### 13.1.1 相关文档

请参阅如下相关文档：

- 《INA21x 电压输出、低侧或高侧测量、双向、零漂移系列分流监控器》（文献编号：SBOS437）
- 《低漂移双向单电源低侧电流感测参考设计》（文献编号：TIDU357）

### 13.2 相关链接

下表列出了快速访问链接。类别包括技术文档、支持与社区资源、工具和软件，以及申请样片或购买产品的快速链接。

表 2. 相关链接

器件	产品文件夹	样片与购买	技术文档	工具和软件	支持和社区
REF2025	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>
REF2030	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>
REF2033	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>
REF2041	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>

### 13.3 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的 [通知我](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 13.4 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [《使用条款》](#)。

**TI E2E™ 在线社区** *TI 的工程师对工程师 (E2E) 社区*。此社区的创建目的在于促进工程师之间的协作。在 [e2e.ti.com](http://e2e.ti.com) 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。

**设计支持** *TI 参考设计支持* 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

### 13.5 商标

E2E is a trademark of Texas Instruments.  
e-Trim is a trademark of Texas Instruments, Inc.  
All other trademarks are the property of their respective owners.

### 13.6 静电放电警告



ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 13.7 术语表

**SLYZ022** — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

## 14 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此产品说明书的浏览器版本，请查阅左侧的导航栏。

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
REF2025AIDDCR	ACTIVE	SOT-23-THIN	DDC	5	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GACM	<a href="#">Samples</a>
REF2025AIDDCT	ACTIVE	SOT-23-THIN	DDC	5	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GACM	<a href="#">Samples</a>
REF2025AISDDCR	ACTIVE	SOT-23-THIN	DDC	5	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1M98	<a href="#">Samples</a>
REF2030AIDDCR	ACTIVE	SOT-23-THIN	DDC	5	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GADM	<a href="#">Samples</a>
REF2030AIDDCT	ACTIVE	SOT-23-THIN	DDC	5	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GADM	<a href="#">Samples</a>
REF2033AIDDCR	ACTIVE	SOT-23-THIN	DDC	5	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GAEM	<a href="#">Samples</a>
REF2033AIDDCT	ACTIVE	SOT-23-THIN	DDC	5	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GAEM	<a href="#">Samples</a>
REF2041AIDDCR	ACTIVE	SOT-23-THIN	DDC	5	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GAFM	<a href="#">Samples</a>
REF2041AIDDCT	ACTIVE	SOT-23-THIN	DDC	5	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GAFM	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

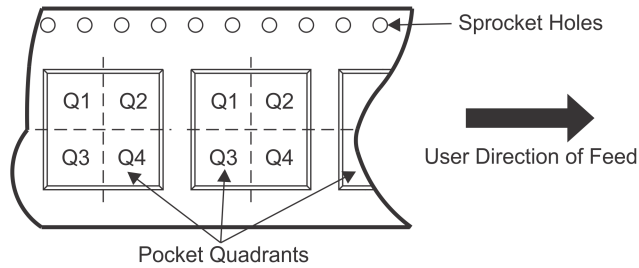
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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
REF2025AIDDCR	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REF2025AIDDCT	SOT-23-THIN	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REF2025AISDDCR	SOT-23-THIN	DDC	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REF2030AIDDCR	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REF2030AIDDCT	SOT-23-THIN	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REF2033AIDDCR	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REF2033AIDDCT	SOT-23-THIN	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REF2041AIDDCR	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REF2041AIDDCT	SOT-23-THIN	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

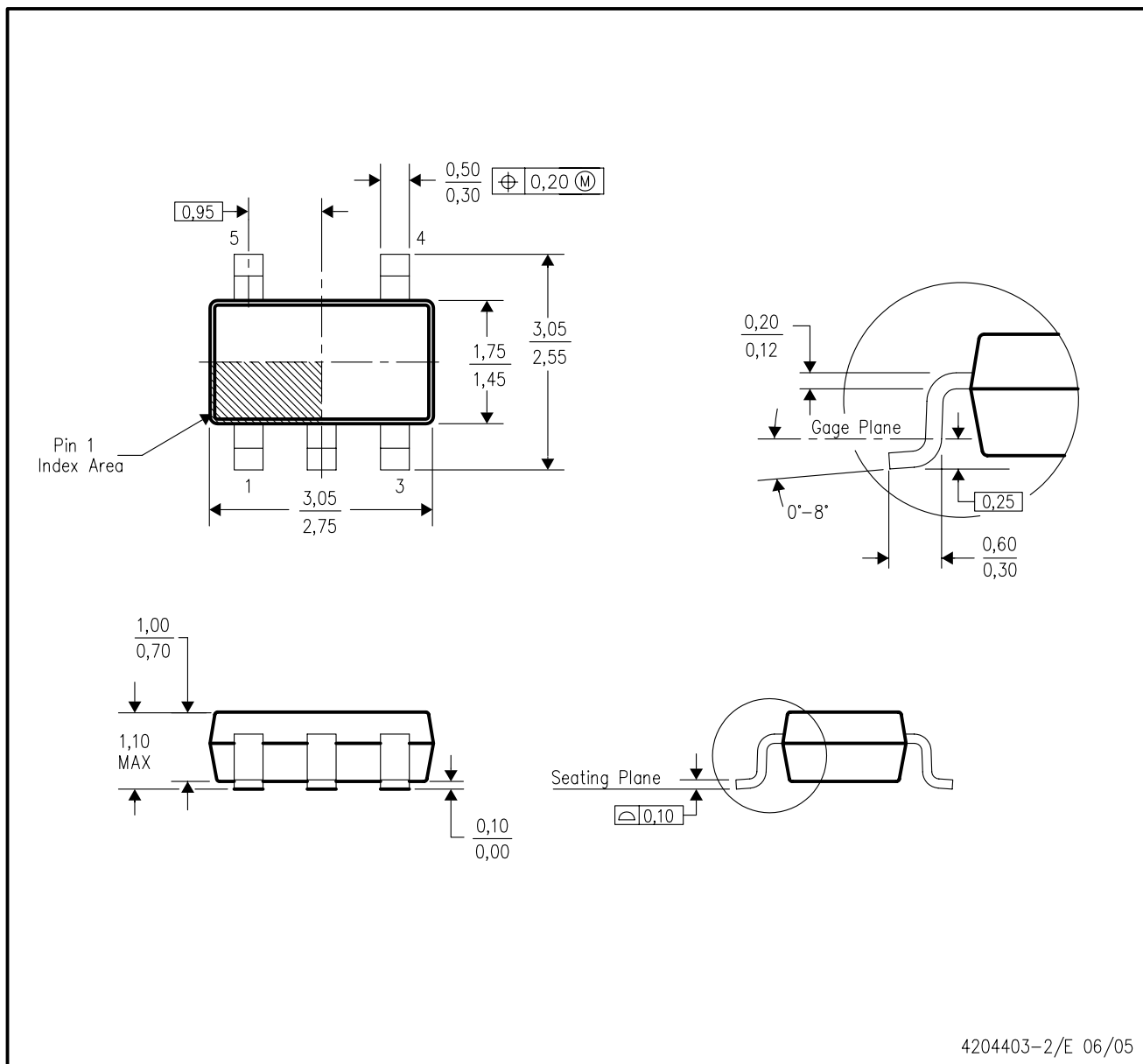
**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
REF2025AIDDCR	SOT-23-THIN	DDC	5	3000	195.0	200.0	45.0
REF2025AIDDCT	SOT-23-THIN	DDC	5	250	195.0	200.0	45.0
REF2025AISDDCR	SOT-23-THIN	DDC	5	3000	195.0	200.0	45.0
REF2030AIDDCR	SOT-23-THIN	DDC	5	3000	195.0	200.0	45.0
REF2030AIDDCT	SOT-23-THIN	DDC	5	250	195.0	200.0	45.0
REF2033AIDDCR	SOT-23-THIN	DDC	5	3000	195.0	200.0	45.0
REF2033AIDDCT	SOT-23-THIN	DDC	5	250	195.0	200.0	45.0
REF2041AIDDCR	SOT-23-THIN	DDC	5	3000	195.0	200.0	45.0
REF2041AIDDCT	SOT-23-THIN	DDC	5	250	195.0	200.0	45.0

DDC (R-PDSO-G5)

PLASTIC SMALL-OUTLINE



4204403-2/E 06/05

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion.
  - D. Falls within JEDEC MO-193 variation AB (5 pin).

## 重要声明和免责声明

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