# Si8941/46/47 Data Sheet

## Isolated Delta-Sigma Modulator for Current Shunt Measurement

The Si8941/46/47 is a galvanically isolated delta-sigma modulator which outputs a digital signal proportional to the voltage level at the input. The low-voltage differential input is ideal for measuring voltage across a current shunt resistor or for any place where a sensor must be isolated from the control system. Low noise, low error, and high precision ensure an accurate measurement of system current.

The output of the Si8941/46/47 comes from a 2nd order delta-sigma modulator. The modulator can be clocked either from an onboard oscillator (Si8946/47) or from an external clock (Si8941). The output is typically digitally filtered by an MCU or FPGA in the system.

The Si8941/46/47 isolated delta-sigma modulator utilizes Skyworks' proprietary isolation technology. It supports up to 5.0 kVrms withstand voltage per UL1577. This technology enables higher performance, reduced variation with temperature and age, tighter part-to-part matching, and longer lifetimes compared to other isolation technologies.

**Applications:**

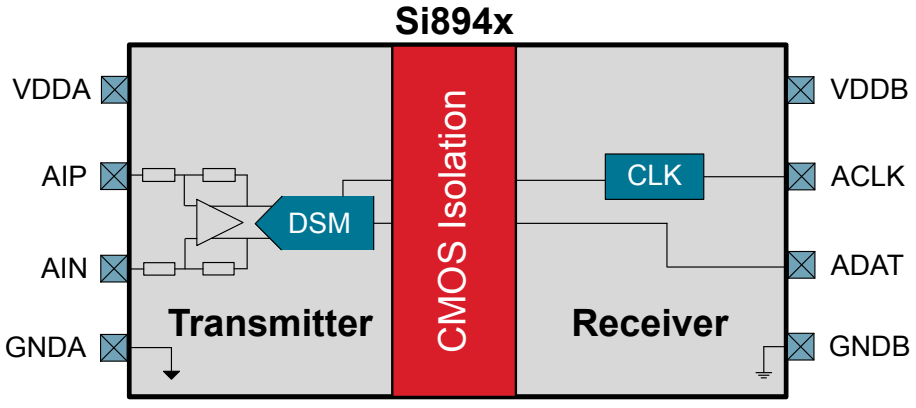
- Industrial, HEV and renewable energy inverters
- AC, Brushless, and DC motor controls and drives
- Variable speed motor control in consumer white goods
- Isolated switch mode and UPS power supplies
- Automotive onboard chargers, battery management systems, and charging stations

**Safety Approvals (pending):**

- UL 1577 recognized
  - Up to 5000 Vrms for 1 minute
- CSA approval
  - IEC 60950-1, 62368-1 (reinforced insulation)
- VDE certification conformity
  - VDE0884 Part 11 (basic/reinforced insulation)
- CQC certification approval
  - GB4943.1-2011

**KEY FEATURES**

- Low voltage differential input
  - ±62.5 mV and ±250 mV options
- Modulator clock options
  - External clock up to 25 MHz (Si8941)
  - 10 MHz internal clock (Si8946)
  - 20 MHz internal clock (Si8947)
- Typical input offset: ±50 µV
- Typical gain error: ±0.05%
- Excellent drift specifications
  - ±0.5 µV/°C typical offset drift
  - ±4 ppm/°C typical gain drift
- Typical 14-bit (ENOB) precision
- High common-mode transient immunity: 75 kV/µs
- Typical SNR: 90 dB
- Typical THD: –97 dB
- Typical nonlinearity: 0.001%
- Auomotive-grade OPNs
  - AIAG-compliant PPAP documentation support
  - IMDS and CAMDS listing support
- Compact packages
  - 8-pin wide body stretched SOIC
  - 8-pin narrow body SOIC
- –40 to 125 °C



# 1. Ordering Guide

**Table 1.1. Si8941-46-47 Ordering Guide[1, 2, 3]**

| Ordering Part Number (OPN) | Automotive OPN[4] | Ordering Options | | | |
|---|---|---|---|---|---|
| | | Specified Input Range | Isolation Rating | Clock | Package Type |
| Si8941AD-IS4 | Si8941AD-AS4 | ±62.5 mV | 5.0 kVrms | Input | WB Stretched SOIC-8 |
| Si8941BD-IS4 | Si8941BD-AS4 | ±250 mV | 5.0 kVrms | Input | WB Stretched SOIC-8 |
| SI8946AD-IS4 | SI8946AD-AS4 | ±62.5 mV | 5.0 kVrms | 10 MHz Output | WB Stretched SOIC-8 |
| SI8946BD-IS4 | SI8946BD-AS4 | ±250 mV | 5.0 kVrms | 10 MHz Output | WB Stretched SOIC-8 |
| SI8947AD-IS4 | SI8947AD-AS4 | ±62.5 mV | 5.0 kVrms | 20 MHz Output | WB Stretched SOIC-8 |
| SI8947BD-IS4 | SI8947BD-AS4 | ±250 mV | 5.0 kVrms | 20 MHz Output | WB Stretched SOIC-8 |
| Si8941AB-IS | Si8941AB-AS | ±62.5 mV | 2.5 kVrms | Input | NB SOIC-8 |
| Si8941BB-IS | Si8941BB-AS | ±250 mV | 2.5 kVrms | Input | NB SOIC-8 |
| SI8946AB-IS | SI8946AB-AS | ±62.5 mV | 2.5 kVrms | 10 MHz Output | NB SOIC-8 |
| SI8946BB-IS | SI8946BB-AS | ±250 mV | 2.5 kVrms | 10 MHz Output | NB SOIC-8 |
| SI8947AB-IS | SI8947AB-AS | ±62.5 mV | 2.5 kVrms | 20 MHz Output | NB SOIC-8 |
| SI8947BB-IS | SI8947BB-AS | ±250 mV | 2.5 kVrms | 20 MHz Output | NB SOIC-8 |

**Note:**

1. All packages are RoHS-compliant.
2. “Si” and “SI” are used interchangeably.
3. AEC-Q100 pending qualification.
4. Automotive-Grade devices ("–A" suffix) are identical in construction materials, topside marking, and electrical parameters to their Industrial-Grade ("–I" suffix) version counterparts. Automotive-Grade products are produced utilizing full automotive process flows and additional statistical process controls throughout the manufacturing flow. The Automotive-Grade part number is included on shipping labels.

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## 2. System Overview

The input to the Si8941/46/47 is designed for low-voltage, differential signals. This is ideal for connection to low-resistance current shunt measurement resistors. The Si8941A/46A/47A has a specified full scale input range of ±62.5 mV, and the Si8941B/46B/47B has a specified full scale input range of ±250 mV. This allows the user to choose low-ohmic resistance value sense resistors to minimize system power loss.

The analog input stage of the Si8941/46/47 is a fully differential amplifier feeding the input of a second-order, delta-sigma (ΔΣ) modulator that digitizes the input signal into a 1-bit output stream. The isolated data output ADAT pin of the converter provides a stream of digital ones and zeros that is synchronous to the ACLK pin. The Si8946/47 clock is generated internally while the Si8941 clock is provided externally. The time average of this serial bit-stream output is proportional to the analog input voltage.

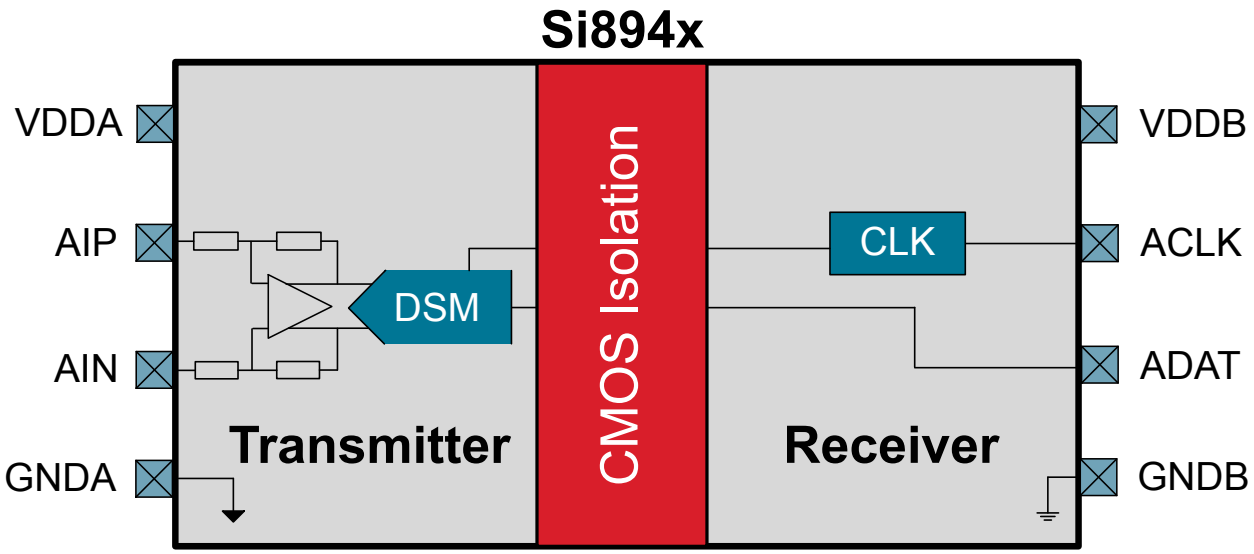


**Figure 2.1. Functional Block Diagram**

### 2.1 Fail-Safe and Low-Power Modes

The Si8941/46/47 implements a fail-safe output when the high-side supply voltage VDDA goes away. The fail-safe output is a steady state Logic 0 on ADAT for the externally clocked Si8941. The fail-safe output is a steady state logic 1 on ADAT for the internally clocked Si8946/47. The clock output ACLK of the Si8946/47 will stop after 256 cycles with a steady state Logic 1. When the supply comes back, the clock will be turned back on and the normal DSM data stream will be output in approximately 250 µs. To differentiate from the failsafe output, a maximum nominal input signal will generate a single one every 128 bits at ADAT.

In addition to the fail-safe output, when a loss of VDDA supply occurs, the part will automatically move into a lower power mode that reduces IDDB current to approximately 1 mA. Similarly, a loss of VDDB supply will reduce IDDA current to approximately 1 mA. When the supply voltage is returned, normal operation begins in approximately 250 µs.

## 2.2 Modulator

The output of the Si8941/46/47 comes from a 2nd order delta-sigma modulator (Figure 2.2 Typical 2nd Order Delta-Sigma Modulator Block Diagram on page 5). The modulator provides 1-bit datastream whose average represents the input analog voltage. 0 V across the inputs is represented at the output by a pulse train that has 50% ones density. Positive specified linear full-scale at the input (e.g., +250 mV for the Si8941B/46B/47B and +62.5 mV for the Si8941A/46A/47A) produces an output datastream that has 89.06% ones density, and negative specified full scale gives an output that has 10.94% ones density. Table Table 2.1 Modulator Output on page 5 shows the values for other input levels and for both full-scale input options of the device.

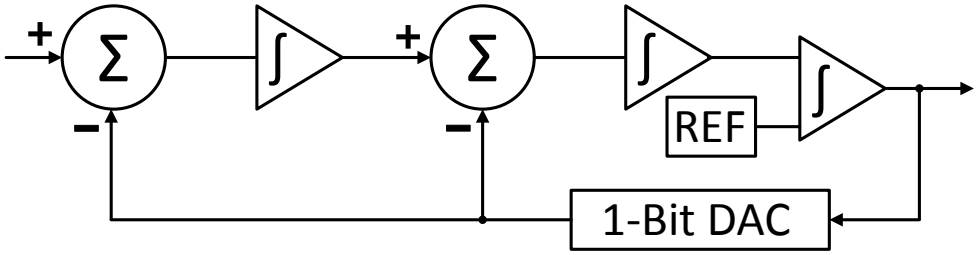


**Figure 2.2. Typical 2nd Order Delta-Sigma Modulator Block Diagram**

**Table 2.1. Modulator Output**

| Differential Input | | Bitstream % Ones |
|---|---|---|
| Si8941A/46A/47A | Si8941B/46B/47B | |
| +62.5 mV | +250 mV | 89.06% |
| +31.25 mV | +125 mV | 69.53% |
| 0 mV | 0 mV | 50% |
| -31.25 mV | -125 mV | 30.47% |
| -62.5 mV | -250 mV | 10.94% |

## 3. Current Sense Application

In the driver circuit presented below, the Si8941/46/47 is used to amplify the voltage across the sense resistor, RSENSE, where it is oversampled and converted into a 1-bit bitstream, then transmitted across the isolation barrier to be processed by the system controller/FPGA. Placing the sense resistor before the load is known as high-side sensing and isolation is needed because the voltage of RSENSE with respect to ground will swing between 0 V and the high voltage rail connected to the drain of Q1.

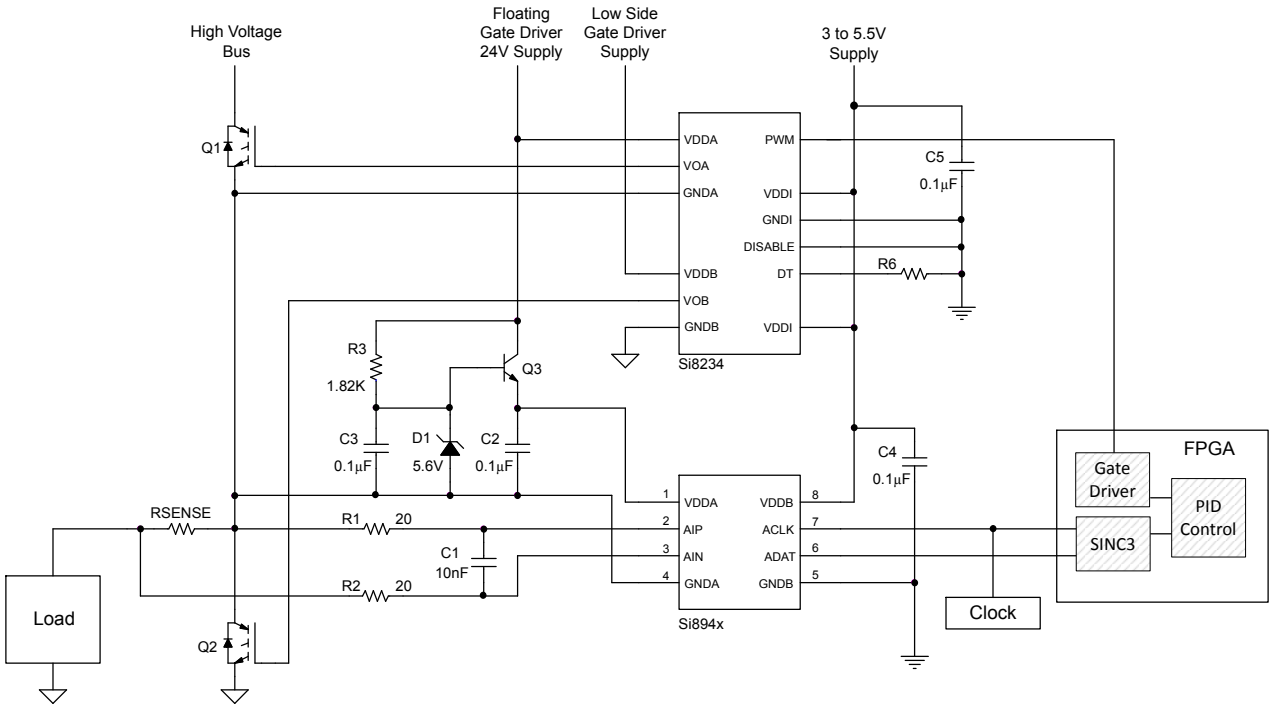


**Figure 3.1. Current Sense Application**

The load in this application can be a motor winding or a similar inductive winding. In a three-phase motor drive application, this circuit would be repeated three times, one for each phase. RSENSE should be a small resistor value to reduce power loss. However, an excessively low resistance will reduce the signal-to-noise ratio of the measurement. Si8941/46/47 offers two specified linear full-scale input options, ±62.5 mV (Si8941A/46A/47A) and ±250 mV (Si8941B/46B/47B), for optimizing the value of RSENSE. Further product ordering options include whether the CLK pin is an input (Si8941) or an output (Si8946/47).

AIP and AIN connections to the RSENSE resistor should be made as close as possible to each end of the RSENSE resistor as trace resistance will add error to the measurement. The input to the Si8941/46/47 is differential, and the PCB traces back to the input pins should run in parallel. This ensures that any large noise transients that occur on the high-voltage side are coupled equally to the AIP and AIN pins and will be rejected by the Si8941/46/47 as a common-mode signal.

The Si8941/46/47 has intrinsic low-pass filtering at approximately 800 kHz. If further input filtering is required, a passive, differential RC low-pass filter can be placed between RSENSE and the input pins. Values of R1 = R2 = 20 Ω and C1 = 10 nF provides a cutoff at approximately 400 kHz. For the lowest gain error, R1 and R2 should always be less than 33 Ω to keep the source impedance sufficiently low compared to the Si8941/46/47 input impedance.

The common-mode voltage of AIN and AIP must be greater than –0.2 V but less than 1 V with respect to GNDA. To meet this requirement, route a trace from the GNDA pin of the Si8941/46/47 to one side of the RSENSE resistor. In this circuit, GNDA, RSENSE, the source of Q1, and the drain of Q2 are connected. The ground of the gate driver (one half of the Skyworks' Si8234 in this example) is also commonly connected to the same node.

The Q1 gate driver has a floating supply of 24 V. Since the input and output of the Si8941/46/47 are galvanically isolated from each other, separate power supplies are necessary on each side. Q3, R3, C3, and D1 make a regulator circuit for powering the input side of the Si8941/46/47 from this floating supply. D1 establishes a voltage of 5.6 V at the base of Q3. R3 is selected to provide a Zener current of 10 mA for D1. C3 provides filtering at the base of Q3, and the emitter output of Q3 provides approximately 5 V to VDDA. C2 is a bypass capacitor for the supply and should be placed at the VDDA pin with its return trace connecting to the GNDA connection at RSENSE.

C4, the local bypass capacitor for the B-side of Si8941/46/47, should be placed closed to VDDB supply pin with its return close to GNDB. The output signal typically goes directly to a digital filter for additional processing. The digital filter may be implemented by a dedicated FPGA in the system or may be a peripheral in the main system controller. The Si8941 expects an external clock to provide

the clock signal for the modulator. That external clock can be provided by the same device that implements the digital filtering or another device that syncs both the modulator and the digital filter. The Si8946/47 generates an internal clock to the digital filter.

# 4. Electrical Specifications

**Table 4.1. Electrical Specifications**

$T_A$ = –40 to +125 °C, AIN = GNDA, SINC3 filter with 256 oversampling ratio and 20 MHz clock; typical specs at 25 °C with VDDA = VDDB = 5 V unless specified differently under Test Condition

| Parameter | | Symbol | Test Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| Input Side Supply Voltage | | VDDA | | 3.0 | | 5.5 | V |
| Input Supply Current | Si8941 | IDDA | VDDA = 3.3 V | 5.7 | 6.9 | 8.2 | mA |
| | Si8946 | IDDA | VDDA = 3.3 V | 5.5 | 6.7 | 8.1 | mA |
| | Si8947 | IDDA | VDDA = 3.3 V | 5.6 | 6.6 | 8.8 | mA |
| Output Side Supply Voltage | | VDDB | | 3.0 | | 5.5 | V |
| Output Supply Current | Si8941 | IDDB | VDDB = 3.3 V | 1.4 | 4 | 4.8 | mA |
| | Si8946 | IDDB | VDDB = 3.3 V | 3.3 | 8 | 6.6 | mA |
| | Si8947 | IDDB | VDDB = 3.3 V | 4.8 | 7.2 | 9.7 | mA |
| **Amplifier Input** | | | | | | | |
| Specified Linear Input Range | Si8941A/46A/47A | VAIP – VAIN | | –62.5 | | 62.5 | mV |
| | Si8941B/46B/47B | | | –250 | | 250 | mV |
| Maximum Input Voltage Before Clipping | Si8941A/46A/47A | VAIP – VAIN | | | ±80 | | mV |
| | Si8941B/46B/47B | | | | ±320 | | mV |
| Common-Mode Operating Range | | VCM | AIN ≠ GNDA | –0.2 | | 1 | V |
| Input Offset | | VOS | $T_A$ = 25 °C, AIP = AIN = 0 | –0.18 | ±0.05 | 0.18 | mV |
| Input Offset Drift | | $VOS_T$ | | –2 | ±0.5 | 2 | µV/°C |
| Gain Error | | $E_G$ | $T_A$ = 25 °C | –0.18 | ±0.05 | 0.18 | % |
| Gain Error Drift | | $E_{GT}$ | | –25 | –4 | 25 | ppm/°C |
| Differential Input Impedance | Si8941A/46A/47A | RIN | | | 6.3 | | kΩ |
| | Si8941B/46B/47B | | | | 21.4 | | kΩ |
| Differential Input Impedance Drift | | $RIN_T$ | | | 850 | | ppm/°C |
| **Dynamic Characteristics** | | | | | | | |
| SNR | Si8941A/46A/47A | SNR | $F_{IN}$ = 5 kHz | 80 | 86 | | dB |
| | Si8941B/46B/47B | | BW = 40 kHz (Si8941/47)<br>BW = 20 kHz (Si8946) | 84 | 90 | | dB |
| Nonlinearity | Si8941A/46A/47A | | $T_A$ = 25 °C | –0.008 | 0.002 | 0.008 | % |
| | Si8941B/46B/47B | | | –0.004 | 0.001 | 0.004 | % |
| Nonlinearity Drift | Si8941/46/47 | | $T_A$ = 25 °C | –0.6 | | 0.6 | ppm/°C |

| Parameter | | Symbol | Test Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| Total Harmonic Distortion | Si8941A/46A/47A | THD | $F_{IN}$ = 5 kHz<br>BW = 40 kHz (Si8941/47)<br>BW = 20 kHz (Si8946) | | –95 | –81 | dB |
| | Si8941B/46B/47B | THD | $F_{IN}$ = 5 kHz<br>BW = 40 kHz (Si8941/47)<br>BW = 20 kHz (Si8946) | | –97 | –81 | dB |
| Power-Supply Rejection Ratio | | PSRR | VDDA at DC | | –100 | | dB |
| | | | VDDA at 100 mV and 10 kHz ripple | | –100 | | dB |
| | | | VDDB at DC | | –100 | | dB |
| | | | VDDB at 100 mV and 10 kHz ripple | | –100 | | dB |
| Common-Mode Transient Immunity | | CMTI | | 50 | 75 | | kV/µs |
| **Digital** | | | | | | | |
| Logic high input threshold (Si8941) | | VIH | | 85% of VDDB | | | V |
| Logic low input threshold (Si8941) | | VIL | | | | 15% of VDDB | V |
| Input hysteresis | | VIHYST | | | 120 | | mV |
| Output load capacitance | | CLOAD | | | 15 | | pF |
| **External Clock (Si8941)** | | | | | | | |
| Clock Frequency | | FCLKIN | | 5 | | 25 | MHz |
| Duty Cycle | | FDUTY | | 45 | 50 | 55 | % |
| Delay to Data Valid | | TDELAY | | | | 23 | ns |
| Data Hold Time | | THOLD | | 6 | | | ns |
| **Internal Clock (Si8946)** | | | | | | | |
| Clock Frequency | | FCLKOUT | $T_A$ = 25 °C | 9.9 | 10 | 10.1 | MHz |
| | | | $T_A$ = –40 °C to 125 °C | 9.8 | 10 | 10.2 | MHz |
| Duty Cycle | | FDUTY | | 45 | 50 | 55 | % |
| Delay to Data Valid | | TDELAY | | | | 60 | ns |
| Data Hold Time | | THOLD | | 40 | | | ns |
| **Internal Clock (Si8947)** | | | | | | | |
| Clock Frequency | | FCLKOUT | $T_A$ = 25 °C | 19.8 | 20 | 20.2 | MHz |
| | | | $T_A$ = –40 °C to 125 °C | 19.6 | 20 | 20.4 | MHz |
| Duty Cycle | | FDUTY | | 45 | 50 | 55 | % |
| Delay to Data Valid | | TDELAY | | | | 30 | ns |
| Data Hold Time | | THOLD | | 20 | | | ns |

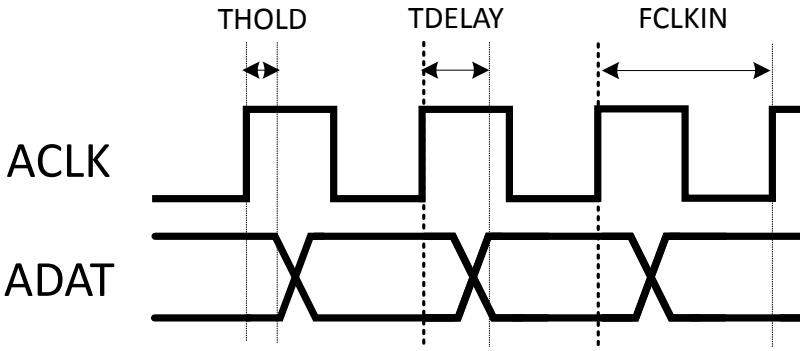


**Figure 4.1. Si8941 Clock Input**

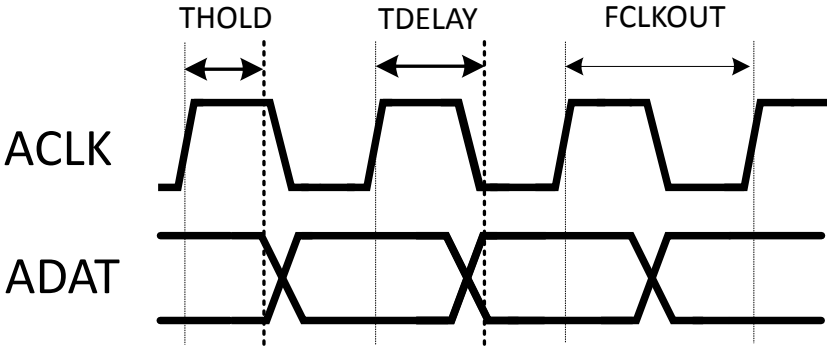


**Figure 4.2. Si8946/47 Clock Output**

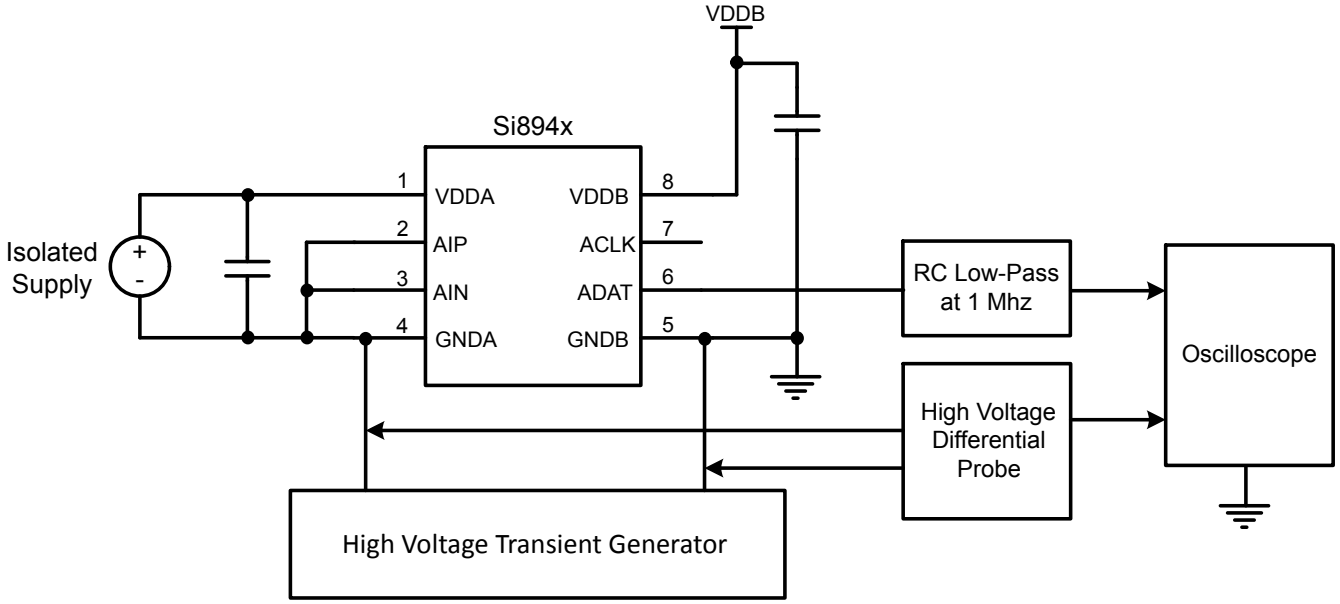


**Figure 4.3. Common-Mode Transient Immunity Characterization Circuit**

**Table 4.2. IEC Safety Limiting Values[1]**

| Parameter | Symbol | Test Condition | Characteristic | Unit |
|---|---|---|---|---|
| Safety Temperature | $T_S$ | | 150 | °C |
| Safety Input Current (WB Stretched SOIC-8) | $I_S$ | $\theta_{JA}$ = 90 °C/W<br>VDD = 5.5 V<br>$T_J$ = 150 °C<br>$T_A$ = 25 °C | 253 | mA |
| | | $\theta_{JA}$ = 90 °C/W<br>VDD = 3.6 V<br>$T_J$ = 150 °C<br>$T_A$ = 25 °C | 386 | mA |
| Safety Input Current (NB SOIC-8) | $I_S$ | $\theta_{JA}$ = 112 °C/W<br>VDD = 5.5 V<br>$T_J$ = 150 °C<br>$T_A$ = 25 °C | 203 | mA |
| | | $\theta_{JA}$ = 112 °C/W<br>VDD = 3.6 V<br>$T_J$ = 150 °C<br>$T_A$ = 25 °C | 310 | mA |
| Safety Input Power (WB Stretched SOIC-8) | $P_S$ | $\theta_{JA}$ = 90 °C/W<br>$T_J$ = 150 °C<br>$T_A$ = 25 °C | 1389 | mW |
| Safety Input Power (NB SOIC-8) | $P_S$ | $\theta_{JA}$ = 112 °C/W<br>$T_J$ = 150 °C<br>$T_A$ = 25 °C | 1116 | mW |
| Device Power Dissipation (WB Stretched SOIC-8) | $P_D$ | | 1.39 | W |
| Device Power Dissipation (NB SOIC-8) | | | 1.12 | W |

**Note:**
1. Maximum value allowed in the event of a failure. Refer to the thermal derating curves below.

**Table 4.3. Thermal Characteristics**

| Parameter | Symbol | WB Stretched SOIC-8 | NB SOIC-8 | Unit |
|---|---|---|---|---|
| IC Junction-to-Air Thermal Resistance | $\theta_{JA}$ | 90 | 112 | °C/W |

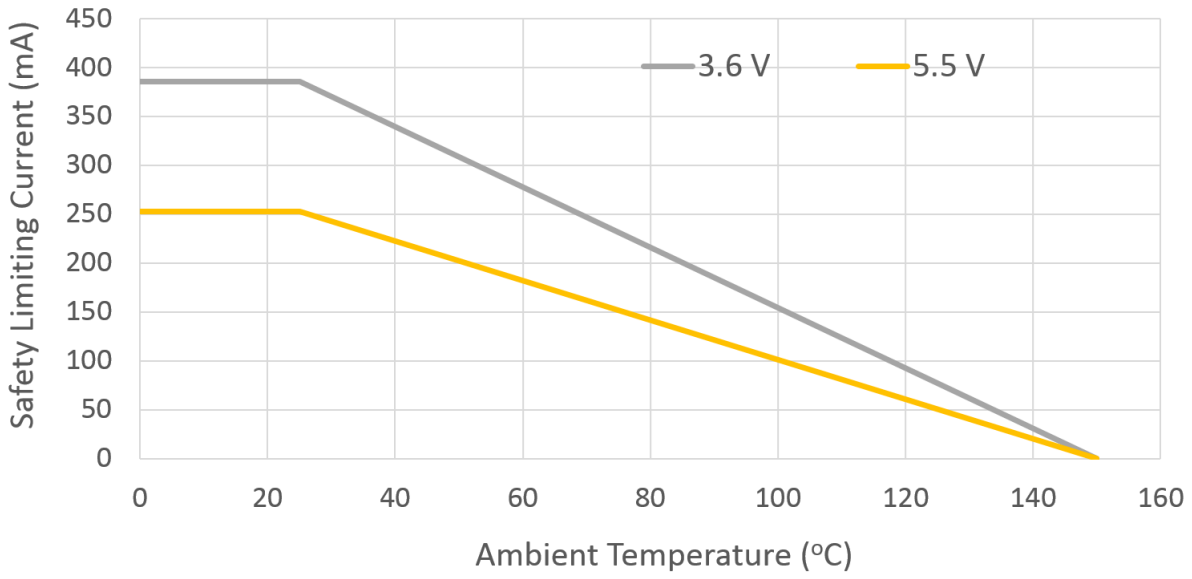


**Figure 4.4. WB Stretched SOIC-8 Thermal Derating Curve for Safety Limiting Current**

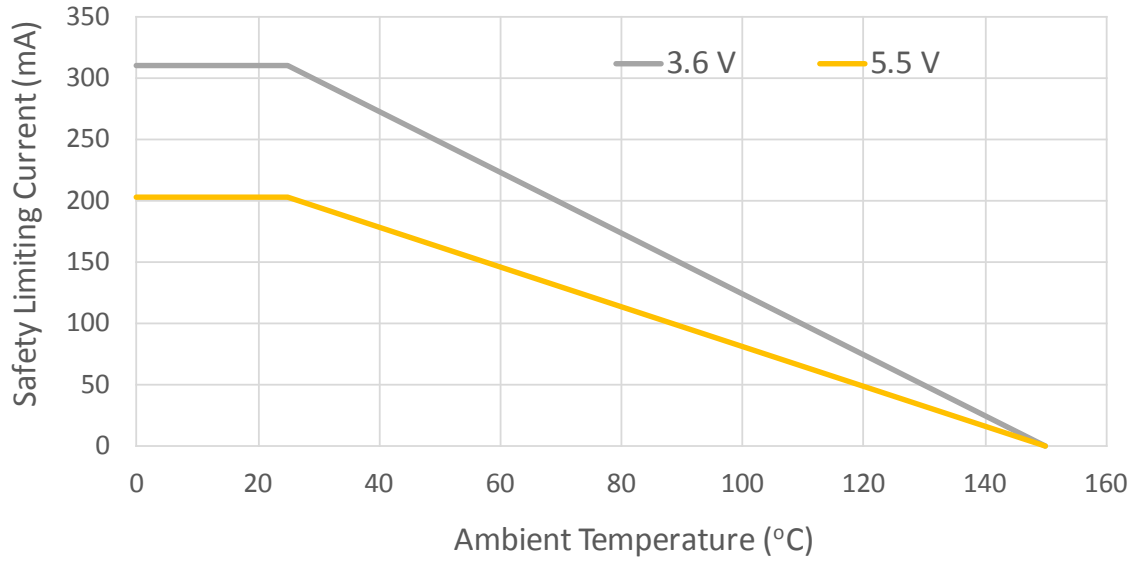


**Figure 4.5. NB SOIC-8 Thermal Derating Curve for Safety Limiting Current**

**Table 4.4. Absolute Maximum Ratings[1]**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Storage Temperature | $T_{STG}$ | –65 | 150 | °C |
| Ambient Temperature Under Bias | $T_A$ | –40 | 125 | °C |
| Junction Temperature | $T_J$ | — | 150 | °C |
| Supply Voltage | VDDA, VDDB | –0.5 | 6.0 | V |
| Input Voltage respect to GNDA | VAIP, VAIN | –0.5 | VDDA+ 0.5 | V |
| Output Sink or Source Current | $I_O$ | — | 5 | mA |
| Total Power Dissipation | $P_T$ | — | 212 | mW |
| Lead Solder Termperature (10 s) | | — | 260 | °C |
| Human Body Model ESD Rating | | 6000 | — | V |
| Capacitive Discharge Model ESD Rating | | 2000 | — | V |
| Maximum Isolation (WB Stretched SOIC-8 Input to Output) (1 s) | | — | 6500 | $V_{RMS}$ |
| Maximum Isolation (NB SOIC-8 package Input to Output) (1 s) | | — | 4500 | $V_{RMS}$ |

**Note:**

1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to conditions as specified in the operational sections of the data sheet.

## 4.1 Regulatory Information

**Table 4.5. Regulatory Information (Pending)[1, 2]**

| |
|---|
| **CSA** |
| The Si8941/46/47 is certified under CSA. For more details, see Master Contract Number 232873. |
| 60950-1, 62368-1: Up to 600 $V_{RMS}$ reinforced insulation working voltage; up to 1000 $V_{RMS}$ basic insulation working voltage. |
| **VDE** |
| The Si8941/46/47 is certified according to VDE 0884-11. For more details, see File 5006301-4880-0001. |
| VDE 0884-11: Up to 1414 $V_{peak}$ for reinforced insulation working voltage. |
| **UL** |
| The Si8941/46/47 is certified under UL1577 component recognition program. For more details, see File E257455. |
| Rated up to 5000 $V_{RMS}$ isolation voltage for basic protection. |
| **CQC** |
| The Si8941/46/47 is certified under GB4943.1-2011. |
| Rated up to 600 $V_{RMS}$ reinforced insulation working voltage; up to 1000 $V_{RMS}$ basic insulation working voltage. |
| **Note:**<br>1. Regulatory Certifications apply to 5 $kV_{RMS}$ rated devices which are production tested to 6.0 $kV_{RMS}$ for 1 sec.<br>2. Regulatory Certifications apply to 2.5 $kV_{RMS}$ rated devices which are production tested to 3.0 $kV_{RMS}$ for 1 sec. |

**Table 4.6. Insulation and Safety-Related Specifications**

| Parameter | Symbol | Test Condition | Value | | Unit |
|---|---|---|---|---|---|
| | | | WB Stretched SOIC-8 | NB SOIC-8 | |
| Nominal External Air Gap (Clearance) | CLR | | 9.0[1] | 4.9 | mm |
| Nominal External Tracking (Creepage) | CPG | | 8.0[1] | 4.01 | mm |
| Minimum Internal Gap (Internal Clearance) | DTI | | 36 | 36 | µm |
| Tracking Resistance | PTI or CTI | IEC60112 | 600 | 600 | V |
| Erosion Depth | ED | | 0.04 | 0.04 | mm |
| Resistance (Input-Output)[2] | $R_{IO}$ | | $10^{12}$ | $10^{12}$ | Ω |
| Capacitance (Input-Output)[2] | $C_{IO}$ | f = 1 MHz | 1 | 1 | pF |

**Note:**
1. The values in this table correspond to the nominal creepage and clearance values. VDE certifies the clearance and creepage limits as x.x mm minimum. UL does not impose a clearance and creepage minimum for component-level certifications. CSA certifies the clearance and creepage limits as 8 mm minimum.
2. To determine resistance and capacitance, the Si8941/46/47 is converted into a 2-terminal device. Pins 1–4 are shorted together to form the first terminal, and pins 5–8 are shorted together to form the second terminal. The parameters are then measured between these two terminals.

**Table 4.7. IEC 60664-1 Ratings**

| Parameter | Test Conditions | Specification | |
|---|---|---|---|
| | | WB Stretched SOIC-8 | NB SOIC-8 |
| Basic Isolation Group | Material Group | I | I |
| Installation Classification | Rated Mains Voltages ≤ 150 $V_{RMS}$ | I-IV | I-IV |
| | Rated Mains Voltages ≤ 300 $V_{RMS}$ | I-IV | I-IV |
| | Rated Mains Voltages ≤ 600 $V_{RMS}$ | I-IV | I-III |

**Table 4.8. VDE 0884-11 Insulation Characteristics[1]**

| Parameter | Symbol | Test Condition | Characteristic | | Unit |
|---|---|---|---|---|---|
| | | | WB Stretched SOIC-8 | NB SOIC8 | |
| Maximum Working Insulation Voltage | $V_{IORM}$ | | 1414 | 560 | V peak |
| Input to Output Test Voltage | $V_{PR}$ | Method b1 ($V_{IORM}$ x 1.875 = $V_{PR}$, 100% Production Test, $t_m$ = 1 sec, Partial Discharge < 5 pC) | 2650 | 1050 | V peak |
| Transient Overvoltage | $V_{IOTM}$ | t = 60 sec | 8000 | 4000 | V peak |
| Surge Voltage | $V_{IOSM}$ | Tested per IEC 60065 with surge voltage using rise/decay time of 1.2 µs/50 µs | 6250 (Tested with 10 kV) | 6250 (Tested with 10 kV) | V peak |
| Pollution Degree (DIN VDE 0110, Table 1) | | | 2 | 2 | Ω |
| Insulation Resistance at $T_S$, $V_{IO}$ = 500 V | $R_S$ | | $>10^9$ | $>10^9$ | Ω |

**Note:**

1. This isolator is suitable for reinforced electrical isolation only within the safety limit data. Maintenance of the safety data is ensured by protective circuits. The Si8941/46/47 provides a climate classification of 40/125/21.

## 4.2 Typical Operating Characteristics

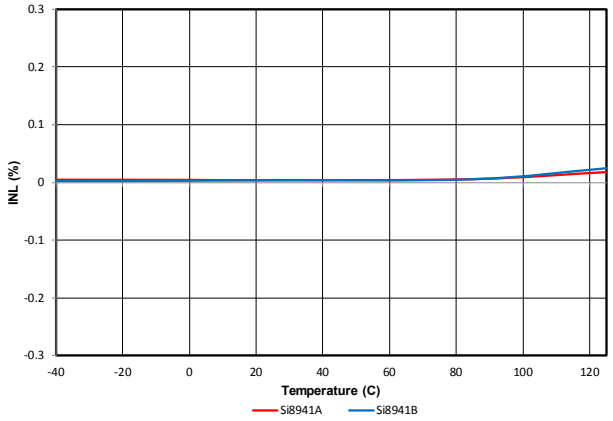


**Figure 4.6. Si8941 Nonlinearity (%) vs. Temperature (°C)**

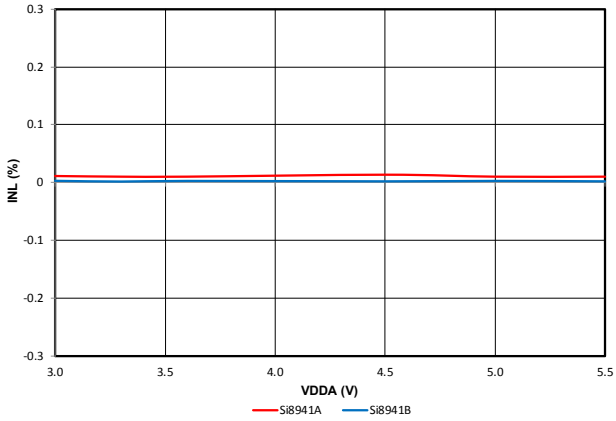


**Figure 4.7. Si8941 Nonlinearity (%) vs. VDDA Supply (V)**

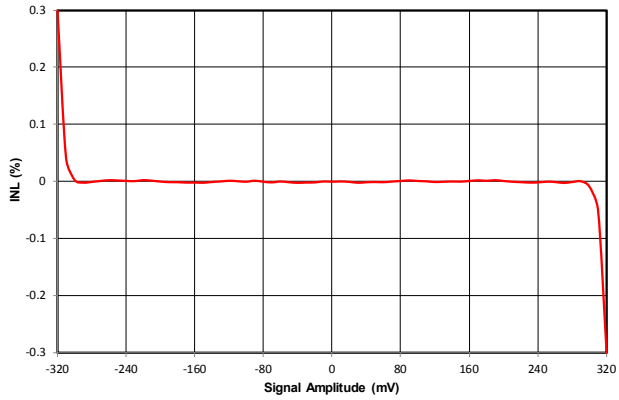


**Figure 4.8. Si8941B Nonlinearity (%) vs. Input Signal Amplitude (mV)**

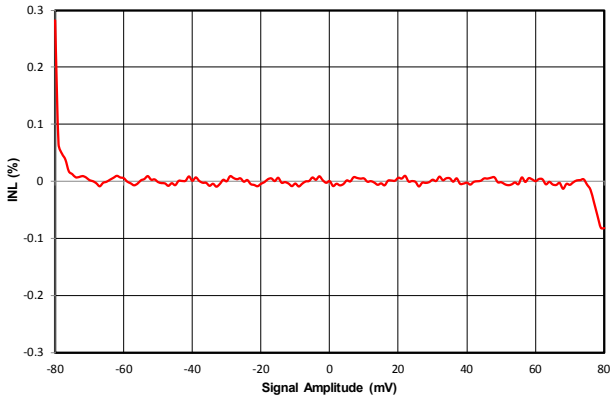


**Figure 4.9. Si8941A Nonlinearity (%) vs. Input Signal Amplitude (mV)**

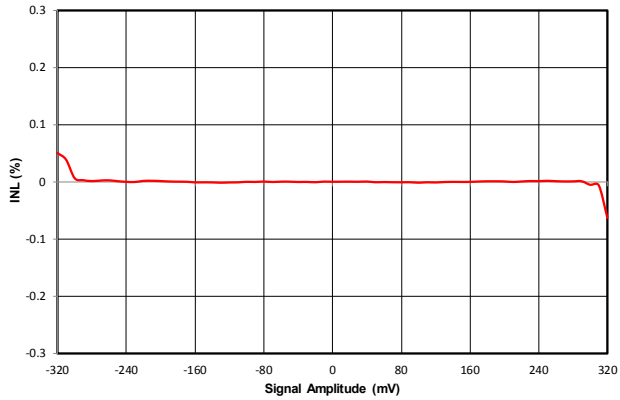


**Figure 4.10. Si8946B Nonlinearity (%) vs. Input Signal Amplitude (mV)**

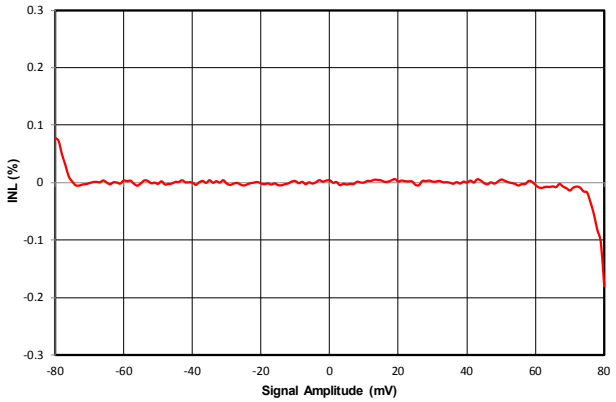


**Figure 4.11. Si8946A Nonlinearity (%) vs. Input Signal Amplitude (mV)**

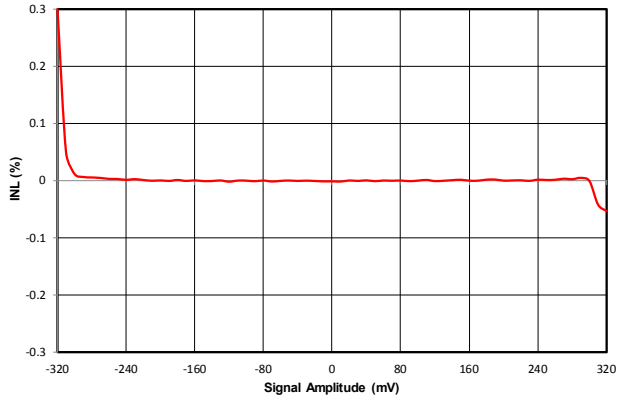


**Figure 4.12. Si8947B Nonlinearity (%) vs. Input Signal Amplitude (mV)**

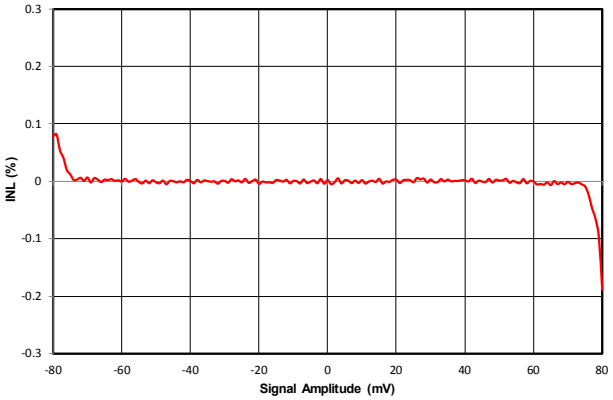


**Figure 4.13. Si8947A Nonlinearity (%) vs. Input Signal Amplitude (mV)**

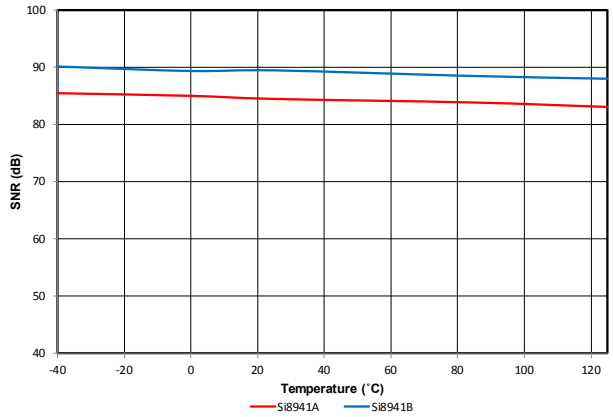


**Figure 4.14. Si8941 Signal-to-Noise Ratio (dB) vs. Temperature (°C)**

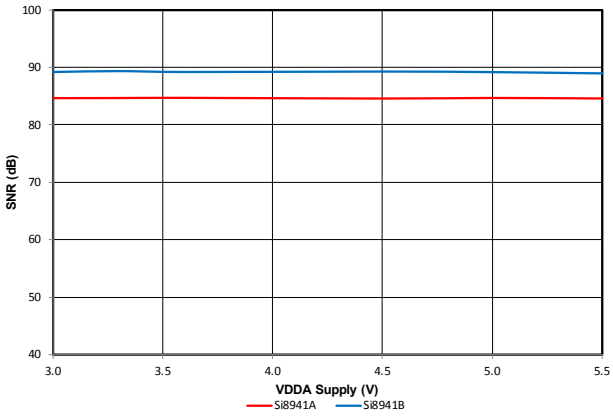


**Figure 4.15. Si8941 Signal-to-Noise Ratio (dB) vs. VDDA Supply (V)**

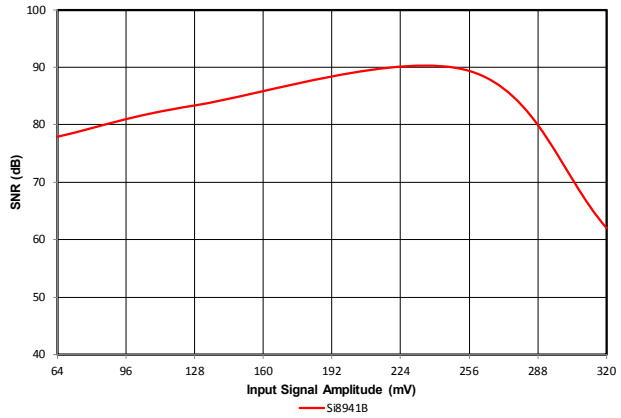


**Figure 4.16. Si8941B Signal-to-Noise Ratio (dB) vs. Input Signal Amplitude (mV)**

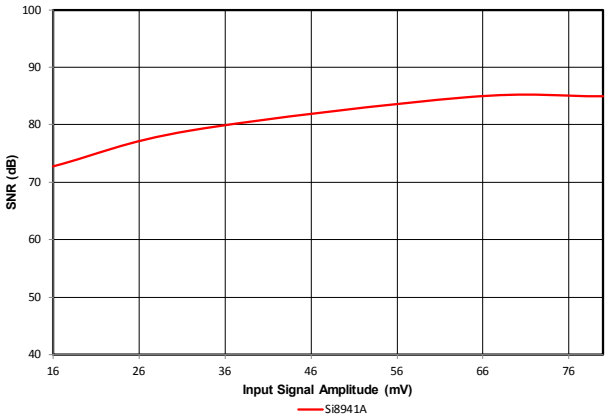


**Figure 4.17. Si8941A Signal-to-Noise Ratio (dB) vs. Input Signal Amplitude (mV)**

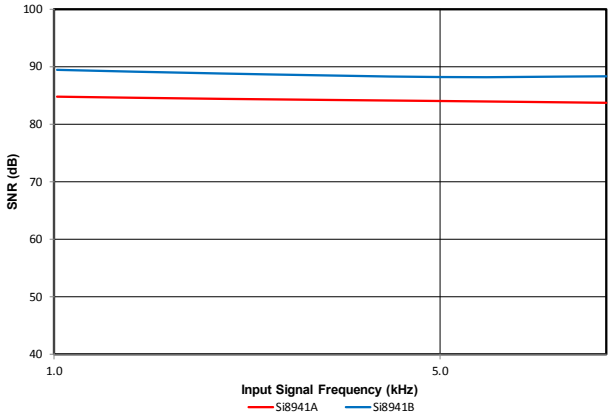


**Figure 4.18. Si8941 Signal-to-Noise Ratio (dB) vs. Input Signal Frequency (kHz)**

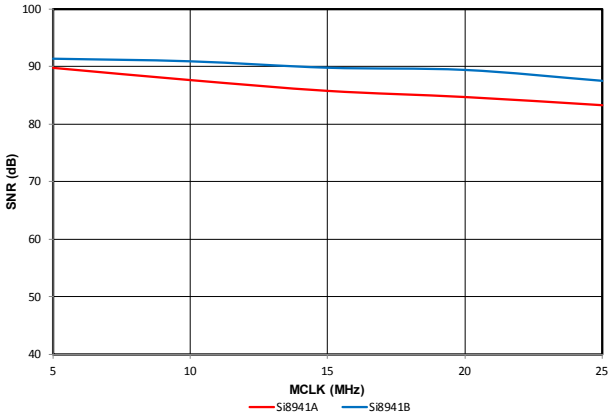


**Figure 4.19. Si8941 Signal-to-Noise Ratio (dB) vs. MCLK (MHz)**

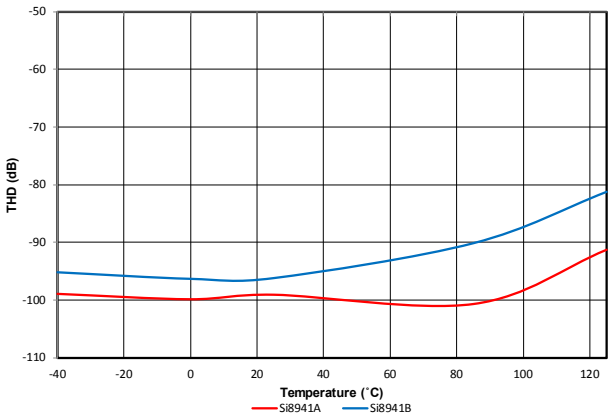


**Figure 4.20. Si8941 Total Harmonic Distortion (dB) vs. Temperature (°C)**

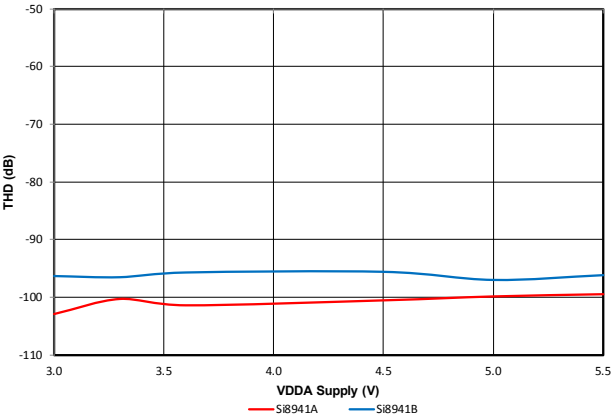


**Figure 4.21. Si8941 Total Harmonic Distortion (dB) vs. VDDA Supply (V)**

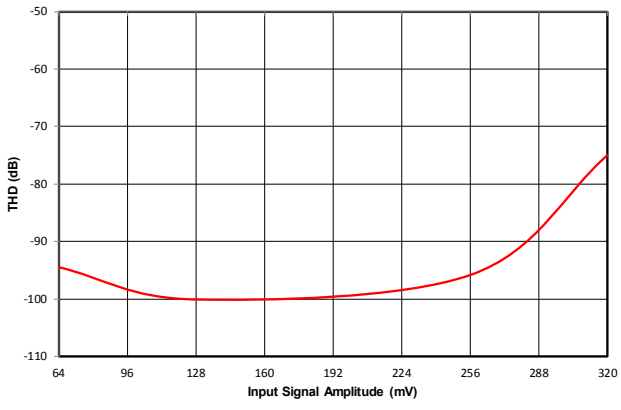


**Figure 4.22. Si8941B Total Harmonic Distortion (dB) vs. Input Signal Amplitude (mV)**

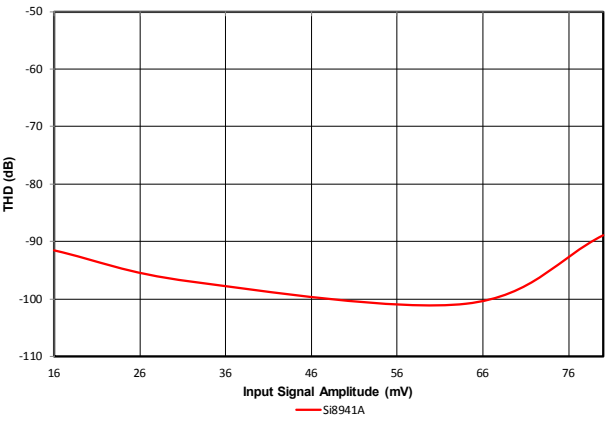


**Figure 4.23. Si8941A Total Harmonic Distortion (dB) vs. Input Signal Amplitude (mV)**

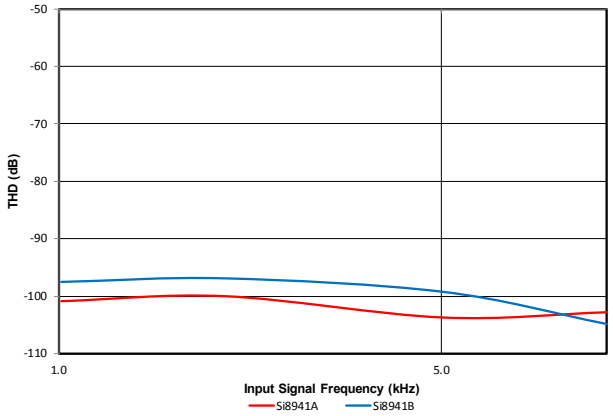


**Figure 4.24. Si8941 Total Harmonic Distortion (dB) vs. Input Signal Frequency (kHz)**

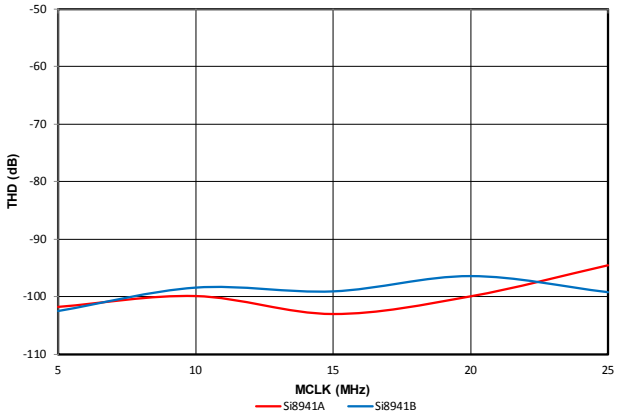


**Figure 4.25. Si8941 Total Harmonic Distortion (dB) vs. MCLK (MHz)**

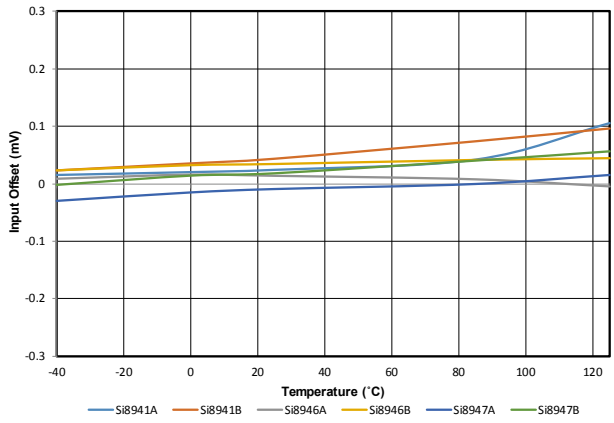


**Figure 4.26. Input Offset (mV) vs. Temperature (°C)**

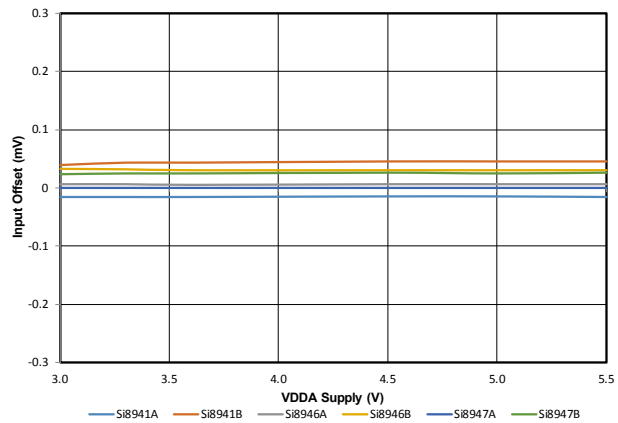


**Figure 4.27. Input Offset (mV) vs. VDDA Supply (V)**

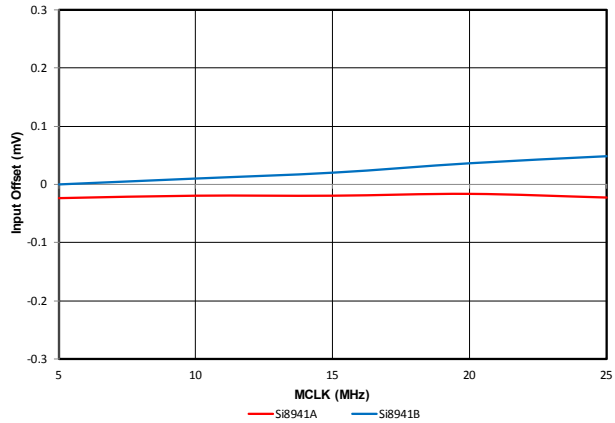


**Figure 4.28. Si8941 Input Offset (mV) vs. MCLK (MHz)**

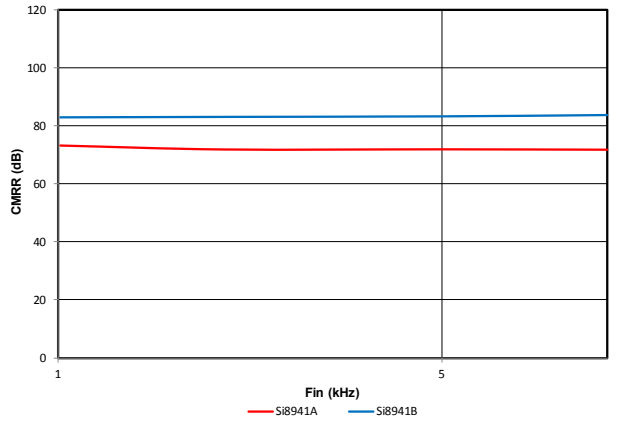


**Figure 4.29. Si8941 Common-Mode Rejection Ratio (dB) vs. Input Signal Frequency (kHz)**

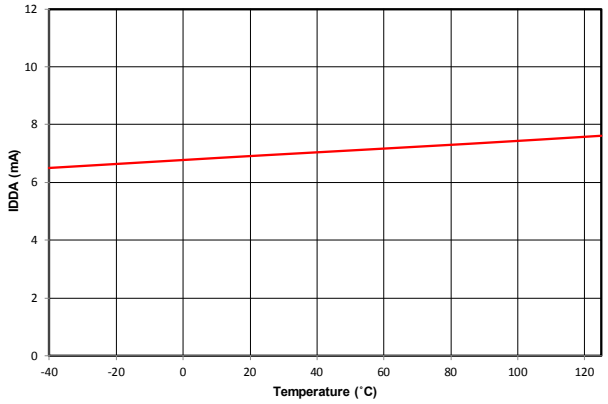


**Figure 4.30. IDDA (mA) vs. Temperature (°C)**

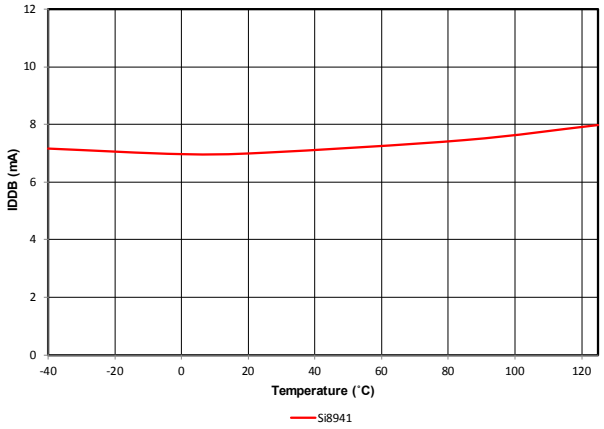


**Figure 4.31. Si8941 IDDB (mA) vs. Temperature (°C)**

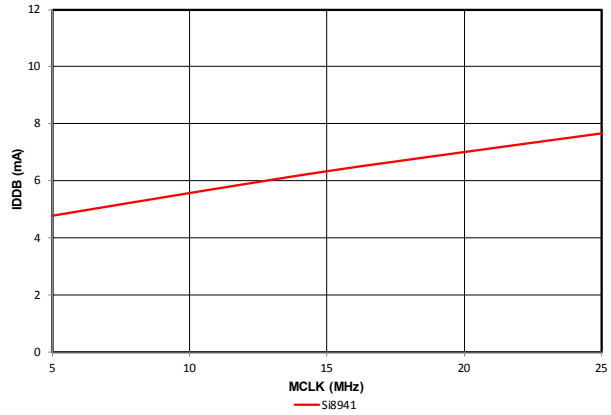


**Figure 4.32. Si8941 IDDB (mA) vs. MCLK (MHz)**

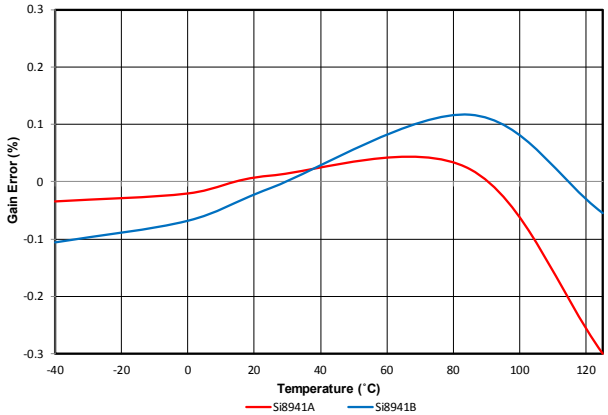


**Figure 4.33. Si8941 Gain Error (%) vs. Temperature (°C)**

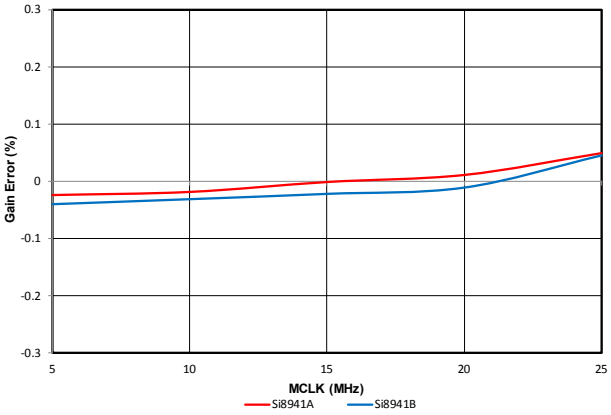


**Figure 4.34. Si8941 Gain Error (%) vs. MCLK (MHz)**

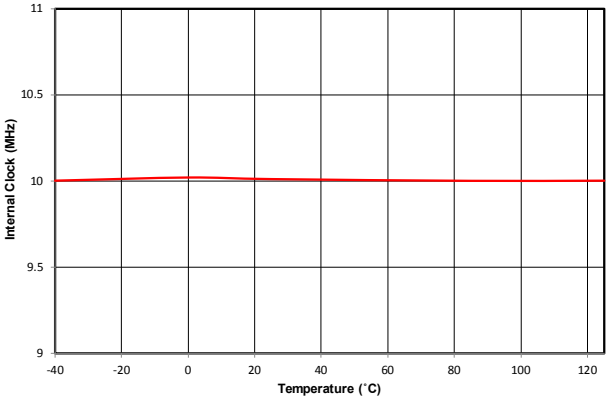


**Figure 4.35. Si8946 Internal Clock Frequency (MHz) vs. Temperature (°C)**

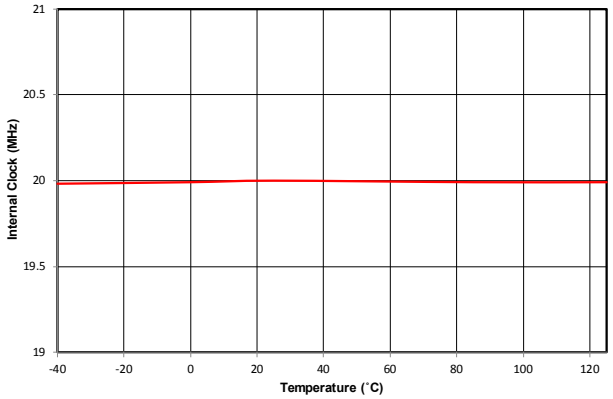


**Figure 4.36. Si8947 Internal Clock Frequency (MHz) vs. Temperature (°C)**

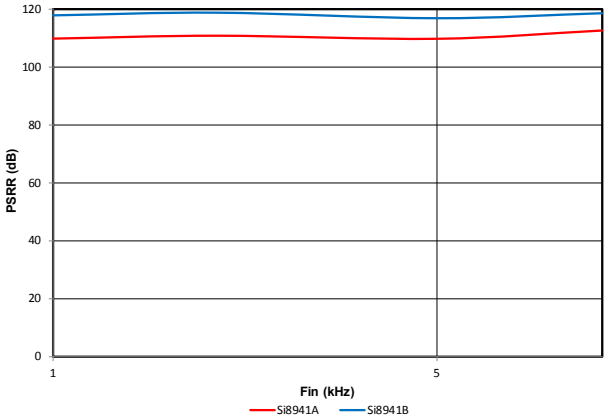


**Figure 4.37. Si8941 Power Supply Rejection Ratio (dB) vs. Input Signal Frequency (kHz)**

# 5. Pin Descriptions

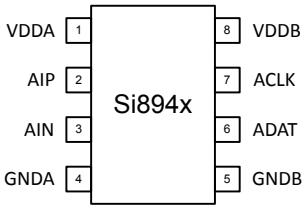


**Table 5.1. Si894x Pin Descriptions**

| Name | Pin Number | Description |
|---|---|---|
| VDDA | 1 | Input side power supply |
| AIP | 2 | Analog input high |
| AIN | 3 | Analog input low |
| GNDA | 4 | Input side ground |
| GNDB | 5 | Output side ground |
| ADAT | 6 | Delta-Sigma modulator data output |
| ACLK | 7 | Delta-Sigma modulator clock (input on Si8941, output on Si8946/47) |
| VDDB | 8 | Output side power supply |

# 6. Packaging

## 6.1 Package Outline: 8-Pin Wide Body Stretched SOIC

The figure below illustrates the package details for the Si8941/46/47 in a 8-Pin Wide Body Stretched SOIC package. The table lists the values for the dimensions shown in the illustration.

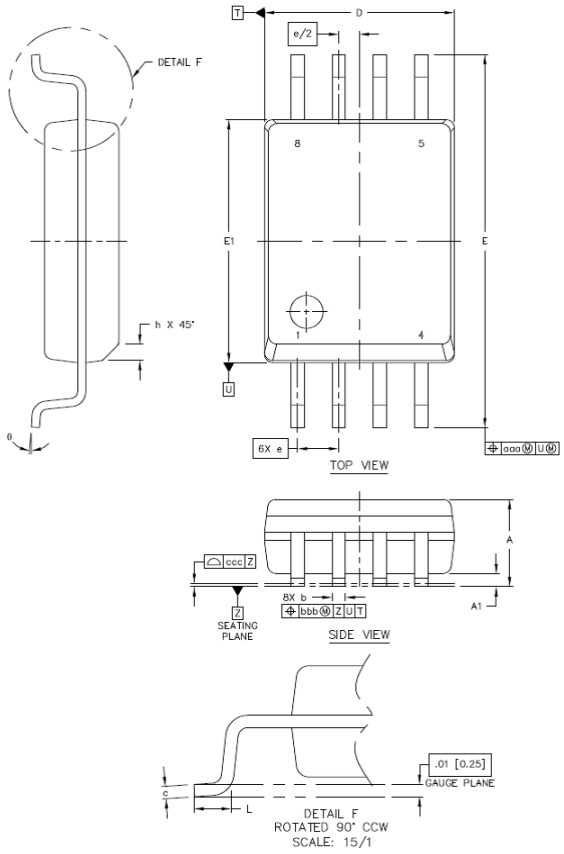


**Figure 6.1. 8-Pin Wide Body Stretched SOIC Package**

**Table 6.1. 8-Pin Wide Body Stretched SOIC Package Diagram Dimensions**

| Dimension | MIN | MAX |
|---|---|---|
| A | 2.49 | 2.79 |
| A1 | 0.36 | 0.46 |
| b | 0.30 | 0.51 |
| c | 0.20 | 0.33 |
| D | 5.74 | 5.94 |
| E | 11.25 | 11.76 |
| E1 | 7.39 | 7.59 |
| e | 1.27 BSC | |
| L | 0.51 | 1.02 |
| h | 0.25 | 0.76 |
| θ | 0° | 8° |

| Dimension | MIN | MAX |
|---|---|---|
| aaa | — | 0.25 |
| bbb | — | 0.25 |
| ccc | — | 0.10 |

**Note:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Recommended reflow profile per JEDEC J-STD-020C specification for small body, lead-free components.

## 6.2 Package Outline: 8-Pin Narrow Body SOIC

The figure below illustrates the package details for the Si8941/46/47 in an 8-Pin Narrow Body SOIC package. The table lists the values for the dimensions shown in the illustration.

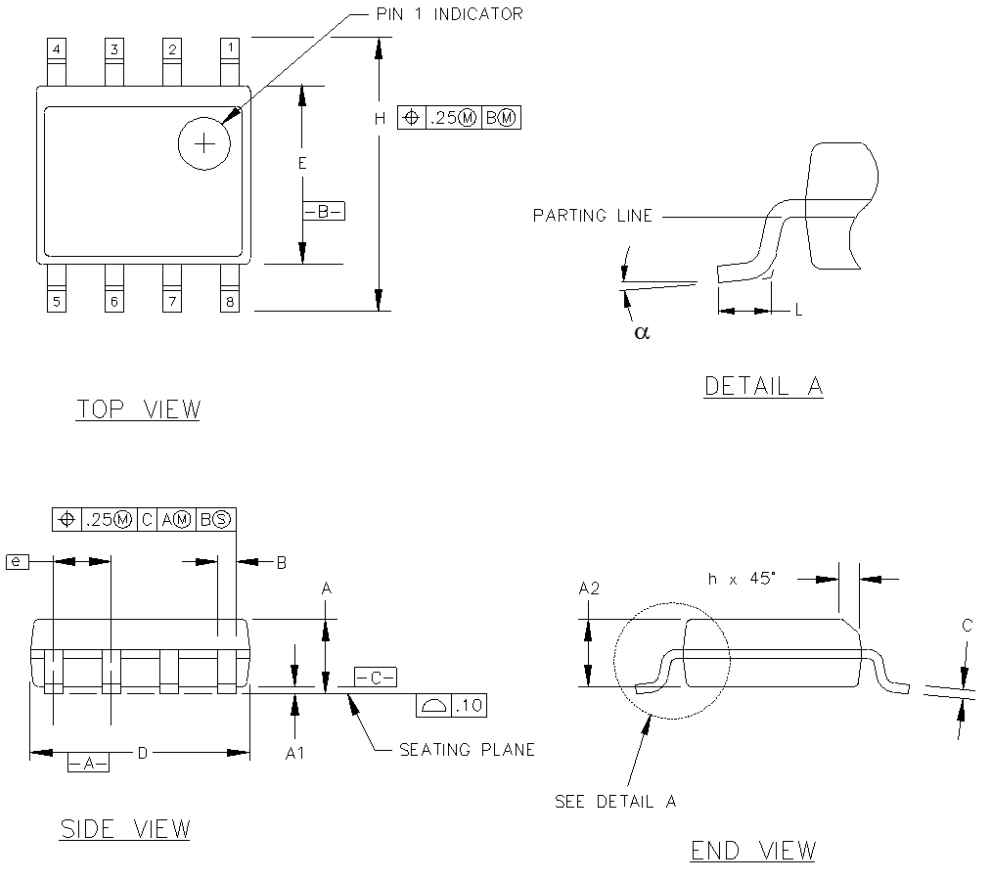


**Figure 6.2. 8-Pin Narrow Body SOIC Package**

**Table 6.2. 8-Pin Narrow Body SOIC Package Diagram Dimensions**

| Dimension | Min | Max |
|---|---|---|
| A | 1.35 | 1.75 |
| A1 | 0.10 | 0.25 |
| A2 | 1.40 REF | 1.55 REF |
| B | 0.33 | 0.51 |
| C | 0.19 | 0.25 |
| D | 4.80 | 5.00 |
| E | 3.80 | 4.00 |
| e | 1.27 BSC | |
| H | 5.80 | 6.20 |
| h | 0.25 | 0.50 |
| L | 0.40 | 1.27 |
| α | 0° | 8° |

| Dimension | Min | Max |
|---|---|---|

**Note:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1982.
3. This drawing conforms to JEDEC Outline MS-012.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020B specification for Small Body Components.

### 6.3 Land Pattern: 8-Pin Wide Body Stretched SOIC

The figure below illustrates the recommended land pattern details for the Si8941/46/47 in a 8-Pin Wide Body Stretched SOIC package. The table lists the values for the dimensions shown in the illustration.

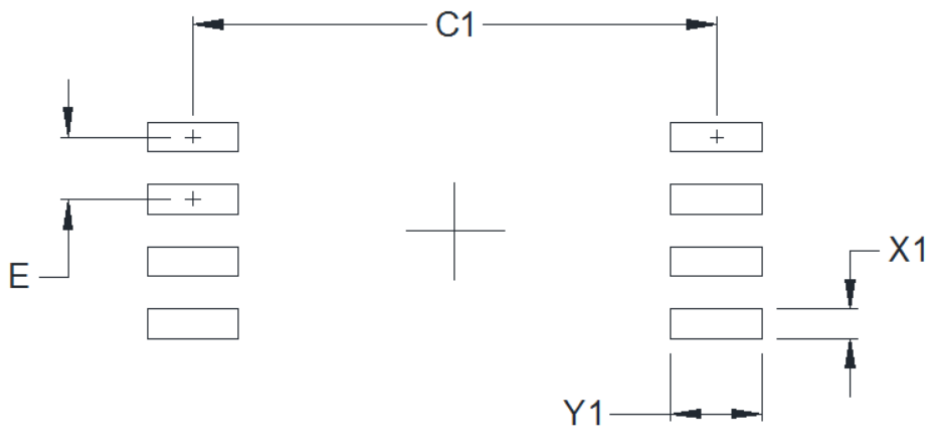


**Figure 6.3. 8-Pin Wide Body Stretched SOIC Land Pattern**

**Table 6.3. 8-Pin Wide Body Stretched SOIC Land Pattern Dimensions[2]**

| Dimension | Feature | (mm) |
|---|---|---|
| C1 | Pad Column Spacing | 10.60 |
| E | Pad Row Pitch | 1.27 |
| X1 | Pad Width | 0.60 |
| Y1 | Pad Length | 1.85 |

**Note:**

**General**

1. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.
2. This Land Pattern Design is based on the IPC-7351 guidelines.

**Solder Mask Design**

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

**Stencil Design**

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pins.

**Card Assembly**

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

### 6.4 Land Pattern: 8-Pin Narrow Body SOIC

The figure below illustrates the recommended land pattern details for the Si8941/46/47 in an 8-Pin Narrow Body SOIC package. The table lists the values for the dimensions shown in the illustration.

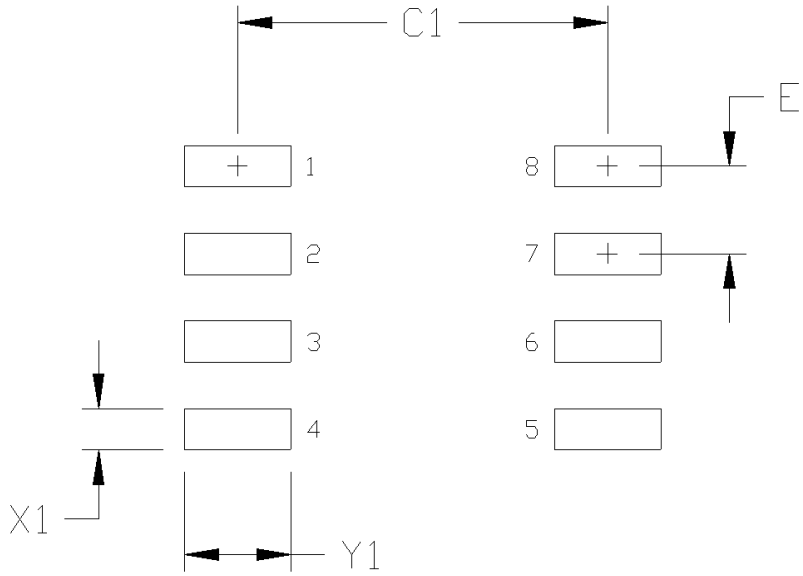


**Figure 6.4. 8-Pin Narrow Body SOIC Land Pattern**

**Table 6.4. 8-Pin Narrow Body SOIC Land Pattern Dimensions**

| Symbol | mm |
|---|---|
| C1 | 5.40 |
| E | 1.27 |
| X1 | 0.60 |
| Y1 | 1.55 |

**Note:**

1. This Land Pattern Design is based on IPC-7351 pattern SOIC127P600X173-8N for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

### 6.5 Top Marking: 8-Pin Wide Body Stretched SOIC

The figure below illustrates the top markings for the Si8941/46/47 in an 8-Pin Wide Body Stretched package. The table explains the top marks shown in the illustration.

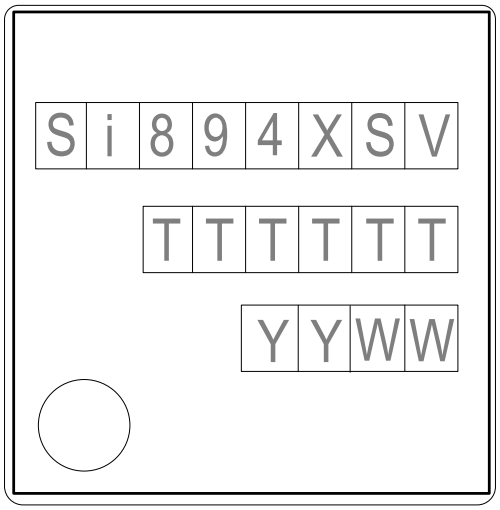


**Figure 6.5. Si894x 8-Pin Wide Body Stretched SOIC Top Marking**

**Table 6.5. 8-Pin Wide Body Stretched SOIC Top Mark Explanation**

| | | |
|---|---|---|
| **Line 1 Marking:** | Customer Part Number | Si8941 or Si8946 or Si8947 Delta-Sigma Modulators<br>X = Clock Source/Speed<br>• 1 = external (Si8941)<br>• 6 = internal 10 MHz (Si8946)<br>• 7 = internal 20 MHz (Si8947)<br>S = Input Range:<br>• A = ±62.5 mV<br>• B = ±250 mV<br>V = Insulation rating:<br>• D = 5.0 kVrms |
| **Line 2 Marking:** | TTTTTT = Mfg Code | Manufacturing Code from the Assembly Purchase Order form. |
| **Line 3 Marking:** | YY = Year<br>WW = Work Week<br>Circle = 43 mils Diameter<br>Left-Justified | Assigned by the Assembly House. Corresponds to the year and work week of the mold date. |

### 6.6 Top Marking: 8-Pin Narrow Body SOIC

The figure below illustrates the top markings for the Si8941/46/47 in an 8-Pin Narrow Body SOIC package. The table explains the top marks shown in the illustration.

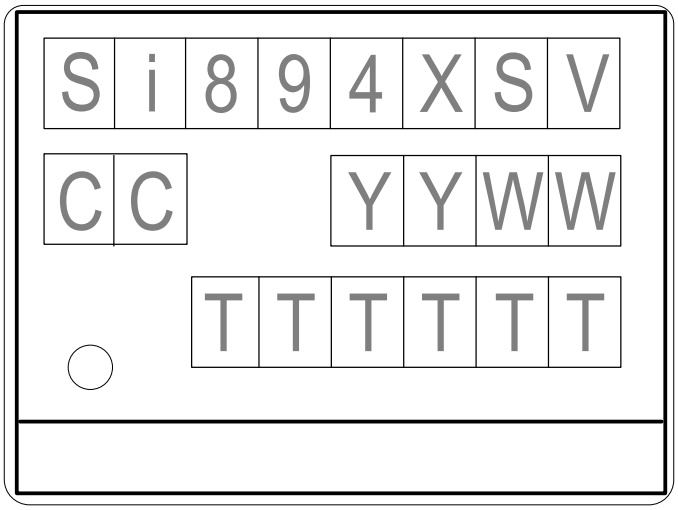


**Figure 6.6. 8-Pin Narrow Body SOIC Top Marking**

**Table 6.6. 8-Pin Narrow Body SOIC Top Mark Explanation**

| | | |
|---|---|---|
| **Line 1 Marking:** | Customer Part Number | Si8941 or Si8946 or Si8947 Delta-Sigma Modulators<br>X = Clock Source/Speed<br>• 1 = external (Si8941)<br>• 6 = internal 10 MHz (Si8946)<br>• 7 = internal 20 MHz (Si8947)<br>S = Input Range:<br>• A = ±62.5 mV<br>• B = ±250 mV<br>V = Insulation rating:<br>• B = 2.5 kVrms |
| **Line 2 Marking:** | CC = Country of Origin ISO Code Abbreviation<br>YY = Year<br>WW = Work Week | Assigned by the Assembly House. Corresponds to the year and work week of the mold date. |
| **Line 3 Marking:** | TTTTTT = Mfg Code<br>Circle = 19.7 mils Diameter<br>Left-Justified | Manufacturing Code from the Assembly Purchase Order form. |

# 7. Revision History

**Revision 0.7**

April, 2021

- Updated Applications and Key Features on front page.
- Updated 4. Electrical Specifications after full characterization.
- Added Automotive OPNs to 1. Ordering Guide.
- Updated Table 4.6 Insulation and Safety-Related Specifications on page 14.
- Numerous clarifications throughout.

**Revision 0.5**

March, 2019

- Updated specifications.
- Added narrow body SOIC package.
- Added timing diagram.

**Revision 0.1**

January, 2018

- Initial release.

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