

## 1.8V/3V SIM Card Power Supply With Level Translator

Check for Samples: [TXS4555](#)

### FEATURES

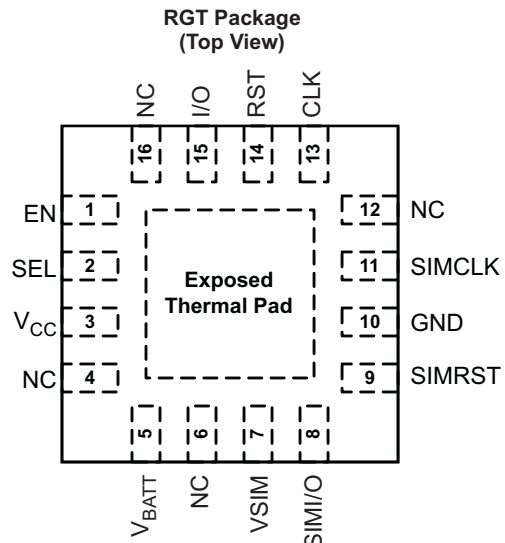
- **Level Translator**
  - $V_{CC}$  Range of 1.65 V to 3.3 V
  - $V_{BATT}$  Range from 2.3 to 5.5V
- **Low-Dropout (LDO) Regulator**
  - 50-mA LDO Regulator With Enable
  - 1.8-V or 2.95-V Selectable Output Voltage
  - 2.3-V to 5.5-V Input Voltage Range
  - Very Low Dropout: 100mV (Max) at 50mA
- **Incorporates Shutdown Feature for the SIM Card Signals According to ISO-7816-3**
- **ESD Protection Exceeds JESD 22**
  - 2000-V Human-Body Model (A114-B)
  - 500-V Charged-Device Model (C101)
  - 8kV HBM for SIM Pins
- **Package**
  - 16-Pin QFN (3 mm x 3 mm)
  - 12-Pin QFN (2mm x 1.7mm)

### DESCRIPTION

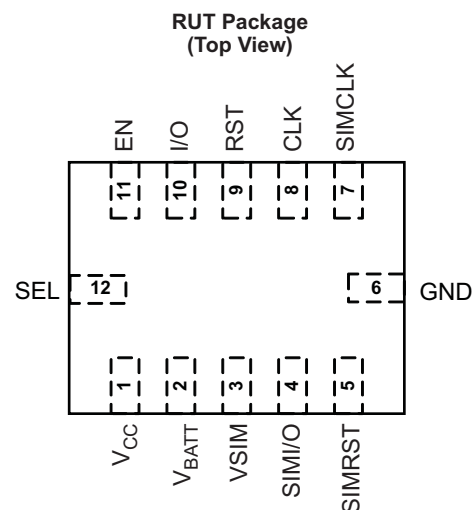
The TXS4555 is a complete Smart Identity Module (SIM) card solution for interfacing wireless baseband processors with a SIM card to store I/O for mobile handset applications. The device complies with ISO/IEC Smart-Card Interface requirements as well as GSM and 3G mobile standards. It includes a high-speed level translator capable of supporting Class-B (2.95 V) and Class-C (1.8 V) interfaces, a low-dropout (LDO) voltage regulator that has output voltages that are selectable between 2.95-V Class-B and 1.8-V Class-C interfaces.

The device has two supply voltage pins.  $V_{CC}$  can be operated over the full range of 1.65 V to 3.3 V and  $V_{BATT}$  from 2.3 to 5.5 V.  $V_{PWR}$  is set to either 1.8 V or 2.95 V and is supplied by an internal LDO. The integrated LDO accepts input voltages as high as 5.5 V and outputs either 1.8 V or 2.95 V at 50 mA to the B-side circuitry and to the external SIM card. The TXS4555 enables system designers to easily interface low-voltage microprocessors to SIM cards operating at 1.8 V or 2.95 V.

The TXS4555 also incorporates shutdown sequence for the SIM card pins based on the ISO 7816-3 specification for SIM cards. Proper shutdown of the SIM card signals helps in prevention of corruption of data during accidental shutdown of the phone. The device also has 8kV HBM protection for the SIM pins and standard 2kV HBM protection for all the other pins.



Note: The Exposed center thermal pad must be connected to Ground



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

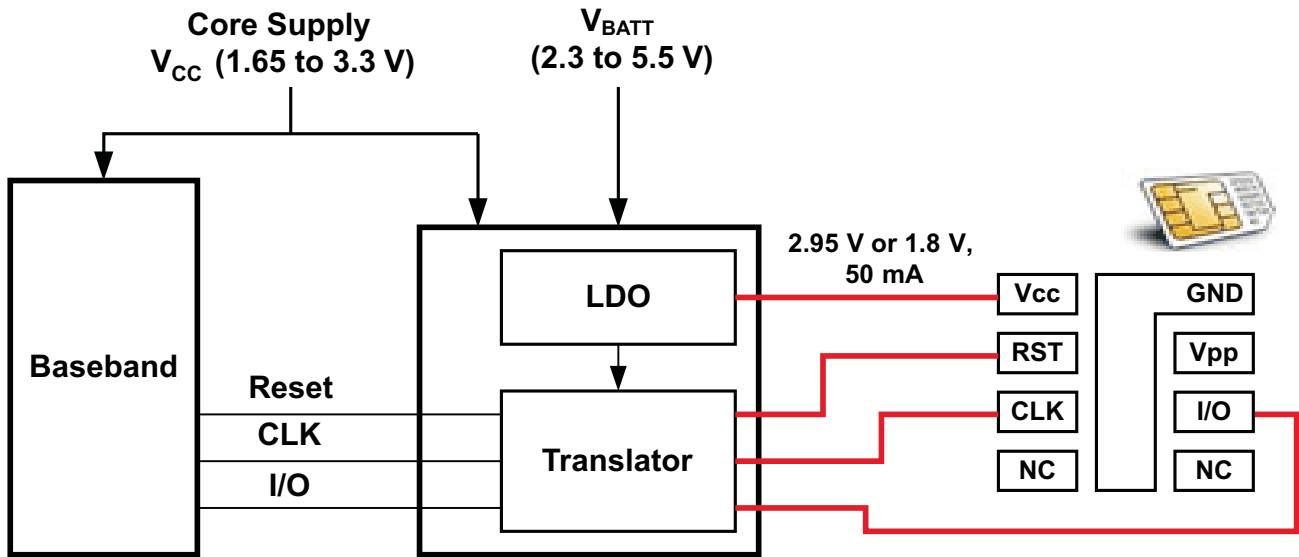


Figure 1. Interfacing with SIM Card

PIN FUNCTIONS

PIN NAME	PIN NO.		TYPE <sup>(1)</sup>	DESCRIPTION
	RGT	RUT		
EN	1	11	I	Enable/disable control input. Pull EN low to place all outputs in Hi-Z state and to disable the LDO. Referenced to VCC.
SEL	2	12	I	Pin to program VSIM value (Low = 1.8V, High = 2.95V)
Vcc	3	1	P	Power supply voltage which powers all A-port I/Os and control inputs
VBATT	5	2	P	Battery power supply
VSIM	7	3	O	SIM card Power-Supply pin (1.8V or 2.95V)
SIM_I/O	8	4	I/O	Bidirectional SIM I/O pin which connected to I/O pin of the SIM card connector
SIM_RST	9	5	O	SIM Reset pin which connects to RESET pin of the SIM card connector
GND	10	6	G	Ground
SIM_CLK	11	7	O	Clock signal pin which connects to CLK pin of the SIM card connector
CLK	13	8	I	Clock signal pin connected from baseband processor
RST	14	9	I	SIM Reset pin connected from baseband processor
I/O	15	10	I/O	Bidirectional SIM I/O pin which connected from baseband processor
NC	4, 6, 12, 16	–	NC	No Connects

(1) G = Ground, I = Input, O = Output, P = Power

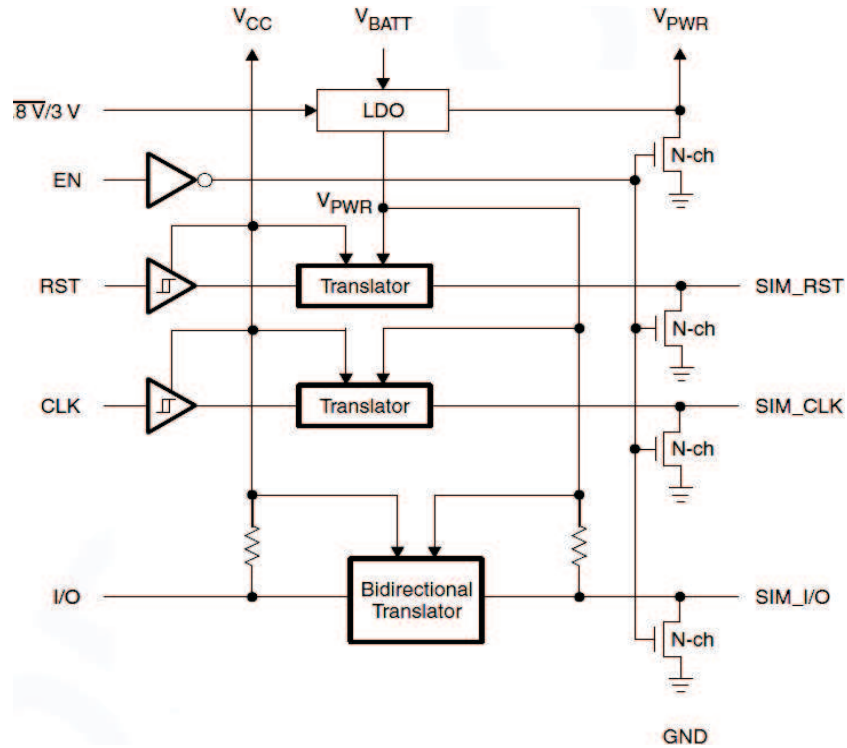


Figure 2. Block Diagram

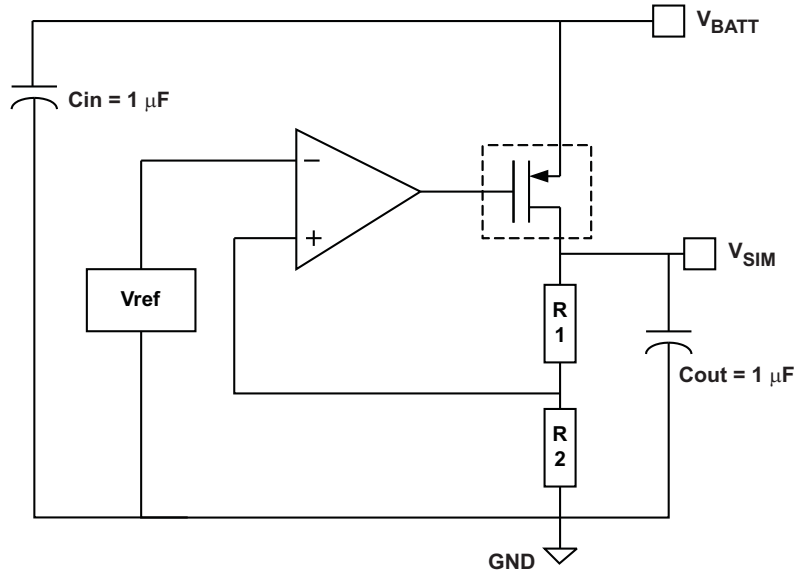
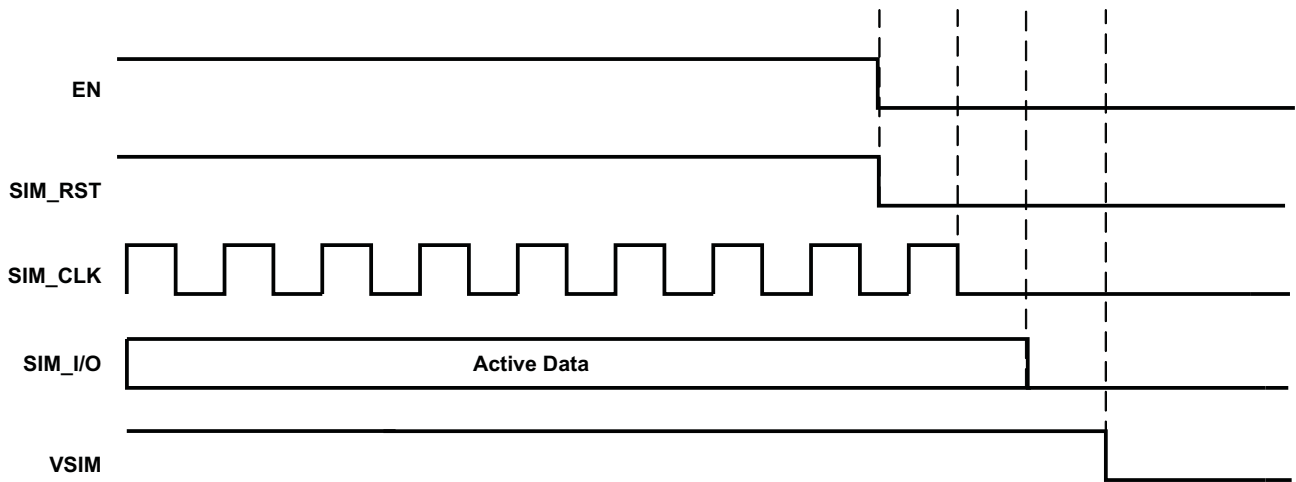


Figure 3. Block Diagram of the LDO



**Figure 4. Shutdown Sequence for SIM\_RST, SIM\_CLK, SIM\_IO and VSIM**

The shutdown sequence for the SIM signals is based on the ISO 7816-3 specification. The shutdown sequence of these signals helps to properly disable these channels and not have any corruption of data accidentally. Also, this is also helpful when the SIM card is present in a hot swap slot and when pulling out the SIM card, the orderly shutdown of these signals help avoid any improper write/corruption of data.

When EN is taken low, the shutdown sequence happens by powering of the SIM\_RST channel. Once that is achieved, SIM\_CLK, SIM\_I/O and VSIM are powered sequentially one by one. There is an internal 2K pull-down value on the SIM pins and helps to pull these channels low. The shutdown time sequence is in the order of a few microseconds. It is important that EN is taken low before VBAT and VCC supplies go low so that the shutdown sequence can be initiated properly.

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

over operating free-air temperature range (unless otherwise noted)

		VALUE		UNIT	
		MIN	MAX		
<b>LEVEL TRANSLATOR</b>					
$V_{CC}$	Supply voltage range	-0.3	4.0	V	
$V_I$	Input voltage range	$V_{CC}$ -port	-0.5	4.6	V
		SIM-port	-0.5	4.6	
		Control inputs	-0.5	4.6	
$V_O$	Voltage range applied to any output in the high-impedance or power-off state	$V_{CC}$ -port	-0.5	4.6	V
		VSIM-port	-0.5	4.6	
		Control inputs	-0.5	4.6	
$V_O$	Voltage range applied to any output in the high or low state	$V_{CC}$ -port	-0.5	4.6	V
		SIM-port	-0.5	4.6	
		Control inputs	-0.5	4.6	
$I_{IK}$	Input clamp current	$V_I < 0$	-50	mA	
$I_{OK}$	Output clamp current	$V_O < 0$	-50	mA	
$I_O$	Continuous output current		±50	mA	
	Continuous current through VCCA or GND		±100	mA	
$T_{stg}$	Storage temperature range	-65	150	°C	
<b>LDO</b>					
$V_{BAT}$	Input voltage range	-0.3	6	V	
$V_{OUT}$	Output voltage range	-0.3	6	V	
	Peak output current		TBD	mA	
	Continuous total power dissipation		TBD		
$T_J$	Junction temperature range	-55	150	°C	
$T_{stg}$	Storage temperature range	-55	150	°C	
	ESD rating (host side)	Human-Body Model (HBM)	2	kV	
		Charged-Device Model (CDM)	500	V	
	ESD rating (SIM side)	Human-Body Model (HBM)	8	kV	

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

**THERMAL INFORMATION**

THERMAL METRIC <sup>(1)</sup>		TXS4555		UNITS
		RGT	RUT	
		16 PINS	12 PINS	
$\theta_{JA}$	Junction-to-ambient thermal resistance	47	87.2	°C/W
$\theta_{JB}$	Junction-to-board thermal resistance	25.12	N/A	
$\psi_{JT}$	Junction-to-top characterization parameter	1.3	1.7	
$\theta_{Jcbot}$	Junction-to-case (bottom) thermal resistance	3.6	n/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

**RECOMMENDED OPERATING CONDITIONS<sup>(1)</sup>**

				MIN	MAX	UNIT
<b>LEVEL TRANSLATOR</b>						
V <sub>CC</sub>	Supply voltage			1.65	3.3	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> - port	EN, SEL, RST, CLK, I/O	V <sub>CC</sub> × 0.7	V <sub>CC</sub>	V
		SIM - port	SIM_I/O	V <sub>sim</sub> × 0.7	V <sub>sim</sub>	
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> - port	EN, SEL, RST, CLK, I/O	0	V <sub>CC</sub> × 0.3	V
		SIM - port	SIM_I/O	0	V <sub>sim</sub> × 0.3	
Δt/Δv	Input transition rise or fall rate				5	ns/V
T <sub>A</sub>	Operating free-air temperature			–40	85	°C

(1) All unused data inputs of the device must be held at V<sub>CC1</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

**ELECTRICAL CHARACTERISTICS – LEVEL TRANSLATOR**

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V <sub>CC</sub>	V <sub>SIM</sub>	MIN	TYP <sup>(1)</sup>	MAX	UNIT
V <sub>OH</sub>	SIM_RST	I <sub>OH</sub> = –1mA	1.65 V to 3.3 V	1.8 V / 2.95 V <sup>(2)</sup>	V <sub>SIM</sub> × 0.8			V
	SIM_CLK	I <sub>OH</sub> = –1mA			V <sub>SIM</sub> × 0.8			
	SIM_I/O	I <sub>OH</sub> = –20 μA			V <sub>SIM</sub> × 0.8			
	I/O	I <sub>OH</sub> = –20 μA			V <sub>CC</sub> × 0.8			
V <sub>OL</sub>	SIM_RST	I <sub>OL</sub> = 1 mA	1.65 V to 3.3 V	1.8 V / 2.95 V <sup>(2)</sup>			V <sub>SIM</sub> × 0.2	V
	SIM_CLK	I <sub>OL</sub> = 1mA					V <sub>SIM</sub> × 0.2	
	SIM_I/O	I <sub>OL</sub> = 1 mA					0.3	
	I/O	I <sub>OL</sub> = 1 mA					0.3	
I <sub>I</sub>	Control inputs	V <sub>I</sub> = EN, 1.8V/3V	1.65 V to 3.3 V	1.8 V / 2.95 V <sup>(2)</sup>			±1	μA
I <sub>CC</sub>	I/O	V <sub>I</sub> = V <sub>CC1</sub> , I <sub>O</sub> = 0	1.65 V to 3.3 V	1.8 V / 2.95 V <sup>(2)</sup>			±5	μA
C <sub>io</sub>	I/O port					8		pF
	SIM ports					4		
C <sub>i</sub>	Control inputs	V <sub>I</sub> = V <sub>CC</sub> or GND				4		pF

(1) All typical values are at T<sub>A</sub> = 25°C.

(2) (Supplied by LDO)

**LDO ELECTRICAL CHARACTERISTICS**

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
V <sub>BAT</sub>	Input voltage		2.3		5.5	V
V <sub>SIM</sub>	Output voltage	Class-B Mode (SEL = V <sub>CC</sub> )	2.85	2.95	3.05	V
		Class-C Mode (SEL = 0)	1.7	1.8	1.9	
V <sub>DO</sub>	Dropout voltage	I <sub>OUT</sub> = 50 mA			100	mV
I <sub>GND</sub>	Ground-pin current	I <sub>OUT</sub> = 0 mA			35	μA
I <sub>SHDN</sub>	Shutdown current (IGND)	V <sub>ENx</sub> ≤ 0.4 V, (V <sub>SIM</sub> + V <sub>DO</sub> ) ≤ V <sub>BAT</sub> ≤ 5.5 V, T <sub>J</sub> = 85°C			3.5	μA
I <sub>OUT(SC)</sub>	Short-circuit current	R <sub>L</sub> = 0 Ω		145		mA
C <sub>OUT</sub>	Output Capacitor			1		μF
PSRR	Power-supply rejection ratio	V <sub>BAT</sub> = 3.25 V, V <sub>SIM</sub> = 1.8 V or 2.95 V, C <sub>OUT</sub> = 1 μF, I <sub>OUT</sub> = 50 mA	f = 1 kHz	50		dB
			f = 10 kHz	40		
T <sub>STR</sub>	Start-up time	V <sub>SIM</sub> = 1.8 V or 2.95 V, I <sub>OUT</sub> = 50 mA, C <sub>OUT</sub> = 1 μF			400	μS
T <sub>J</sub>	Operating junction temperature		–40		125	°C

(1) All typical values are at T<sub>A</sub> = 25°C.

## GENERAL ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R <sub>I/OPU</sub>	I/O pull-up		16	20	24	kΩ
R <sub>SIMPU</sub>	SIM_I/O pull-up		10	14	18	kΩ
R <sub>SIMPD</sub>	SIM_I/O pull-down	Active pull-downs are connected to the VSIM regulator output to the SIM_CLK, SIM_RST, SIM_I/O when EN = 0			3	kΩ

## SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V <sub>CC</sub> = 1.8 V ± 0.15 V		UNIT
			MIN	MAX	
<b>VSIM = 1.8 V or 2.95 V SUPPLIED BY INTERNAL LDO</b>					
t <sub>rA</sub>	SIM_I/O	c <sub>L</sub> = 50 pF			1 μs
t <sub>rB</sub>	SIM_RST				1 μs
	SIM_CLK				18 ns
	SIM_I/O				1 us
f <sub>max</sub>	SIM_CLK				25 MHz
Duty Cycle	SIM_CLK			40%	60%

## OPERATING CHARACTERISTICS

 T<sub>A</sub> = 25°C, V<sub>SIM</sub> = 1.8 V

PARAMETER		TEST CONDITIONS	V <sub>CC</sub> TYP	UNIT
			1.8 V	
C <sub>pdA</sub> <sup>(1)</sup>	Class B	C <sub>L</sub> = 0, f = 5 MHz, t <sub>r</sub> = t <sub>f</sub> = 1 ns	13	pF
	Class C		11	

(1) Power dissipation capacitance per transceiver.

TYPICAL CHARACTERISTICS

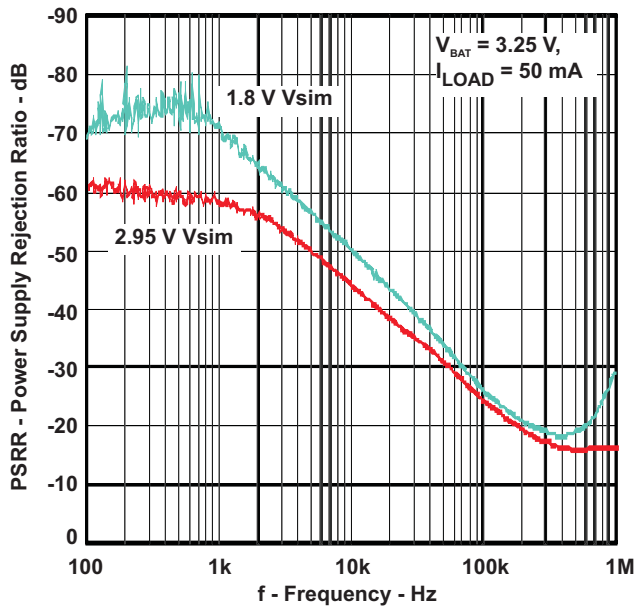


Figure 5. PSRR

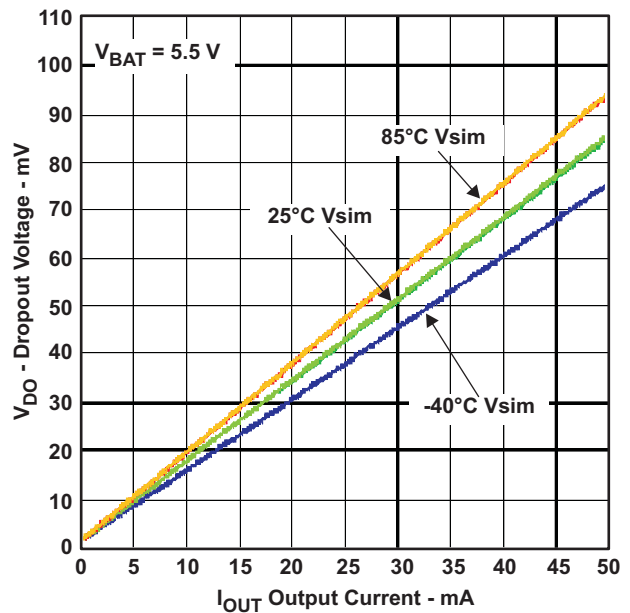


Figure 6. Dropout Voltage vs Output Current

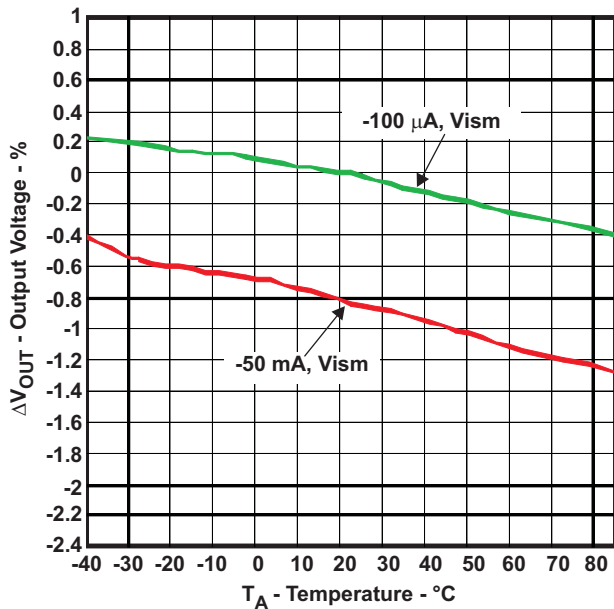


Figure 7. Output Voltage vs Temperature, Class-B/C

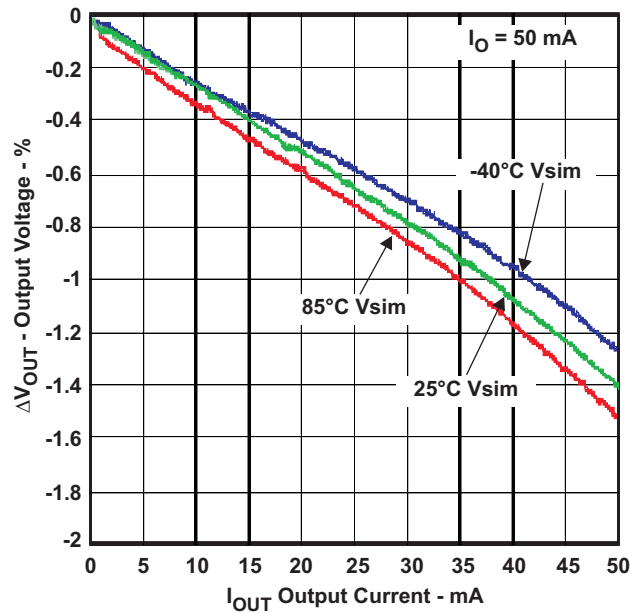
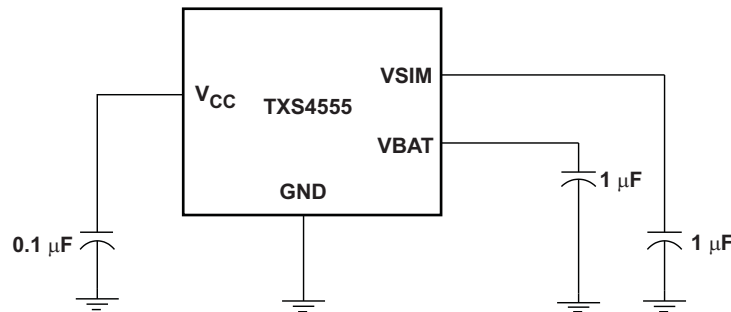


Figure 8. Load Regulation, I<sub>OUT</sub> = 50 mA, Class-C

## APPLICATION INFORMATION

The LDO's included on the TXS4555 achieve ultra-wide bandwidth and high loop gain, resulting in extremely high PSRR at very low headroom ( $V_{BAT} - V_{SIM}$ ). The TXS4555 provides fixed regulation at 1.8V or 2.95V. Low noise, enable, low ground pin current make it ideal for portable applications. The device offers sub-bandgap output voltages, current limit and thermal protection, and is fully specified from  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ .



**Figure 9. Typical Application Circuit for TXS4555**

### INPUT AND OUTPUT CAPACITOR REQUIREMENTS

It is good analog design practice to connect a  $1.0\ \mu\text{F}$  low equivalent series resistance (ESR) capacitor across the input supply (VBAT) near the regulator. Also, a  $0.1\ \mu\text{F}$  is required for the logic core supply (VDDIO).

This capacitor will counteract reactive input sources and improve transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated or if the device is located several inches from the power source. The LDO's are designed to be stable with standard ceramic capacitors of values  $1.0\ \mu\text{F}$  or larger. X5R- and X7R-type capacitors are best because they have minimal variation in value and ESR over temperature. Maximum ESR should be  $< 1.0\ \Omega$ .

### OUTPUT NOISE

In most LDO's, the bandgap is the dominant noise source. To improve ac performance such as PSRR, output noise, and transient response, it is recommended that the board be designed with separate ground planes for  $V_{IN}$  and  $V_{OUT}$ , with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the bypass capacitor should connect directly to the GND pin of the device.

### INTERNAL CURRENT LIMIT

The TXS4555 internal current limit helps protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of output voltage. For reliable operation, the device should not be operated in a current limit state for extended periods of time.

The PMOS pass element in the TXS4555 has a built-in body diode that conducts current when the voltage at VSIM exceeds the voltage at VBAT. This current is not limited, so if extended reverse voltage operation is anticipated, external limiting may be appropriate.

### DROPOUT VOLTAGE

The TXS4555 uses a PMOS pass transistor to achieve low dropout. When  $(V_{BAT} - V_{SIM})$  is less than the dropout voltage ( $V_{DO}$ ), the PMOS pass device is in its linear region of operation and the input-to-output resistance is the  $R_{DS(ON)}$  of the PMOS pass element.  $V_{DO}$  will approximately scale with output current because the PMOS device behaves like a resistor in dropout.

### STARTUP

The TXS4555 uses a quick-start circuit which allows the combination of very low output noise and fast start-up times.

## TRANSIENT RESPONSE

As with any regulator, increasing the size of the output capacitor reduces over/undershoot magnitude but increases duration of the transient response.

## MINIMUM LOAD

The TXS4555 is stable and well-behaved with no output load. Traditional PMOS LDO regulators suffer from lower loop gain at very light output loads. The TXS4555 employs an innovative low-current mode circuit to increase loop gain under very light or no-load conditions, resulting in improved output voltage regulation performance down to zero output current.

## THERMAL INFORMATION

### Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately +160°C, allowing the device to cool. When the junction temperature cools to approximately +140°C the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage because of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat sink. For reliable operation, junction temperature should be limited to +125°C maximum. To estimate the margin of safety in a complete design (including heat sink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least +35°C above the maximum expected ambient condition of your particular application. This configuration produces a worst-case junction temperature of +125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TXS4555 has been designed to protect against overload conditions. It was not intended to replace proper heat sinking. Continuously running the TXS4555 into thermal shutdown will degrade device reliability.

## REVISION HISTORY

<b>Changes from Revision A (March 2011) to Revision B</b>	<b>Page</b>
• Removed Ordering Information table. ....	<a href="#">2</a>
• Updated $V_{IH}$ and $V_{IL}$ to specify additional information. ....	<a href="#">6</a>

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TXS4555RGTR	ACTIVE	VQFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ZUT	<a href="#">Samples</a>
TXS4555RUTR	ACTIVE	UQFN	RUT	12	3000	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	69R	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

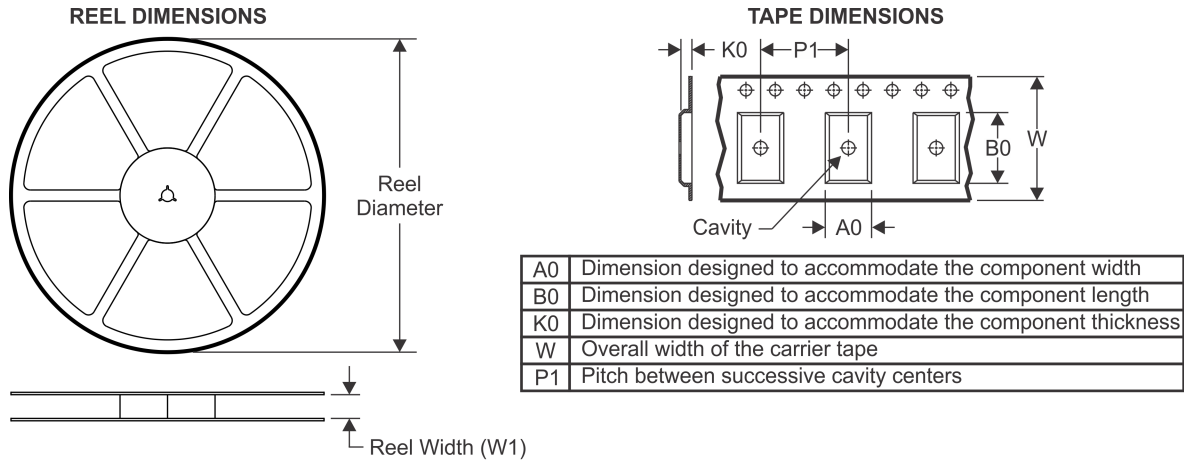
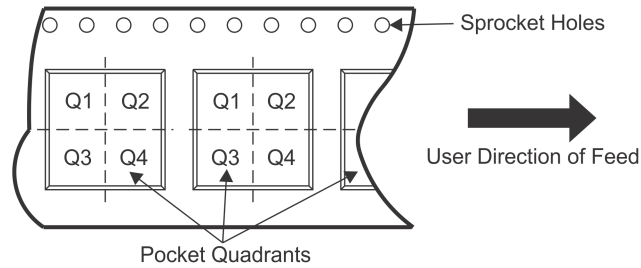
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TXS4555RGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TXS4555RUTR	UQFN	RUT	12	3000	180.0	8.4	1.95	2.3	0.75	4.0	8.0	Q1

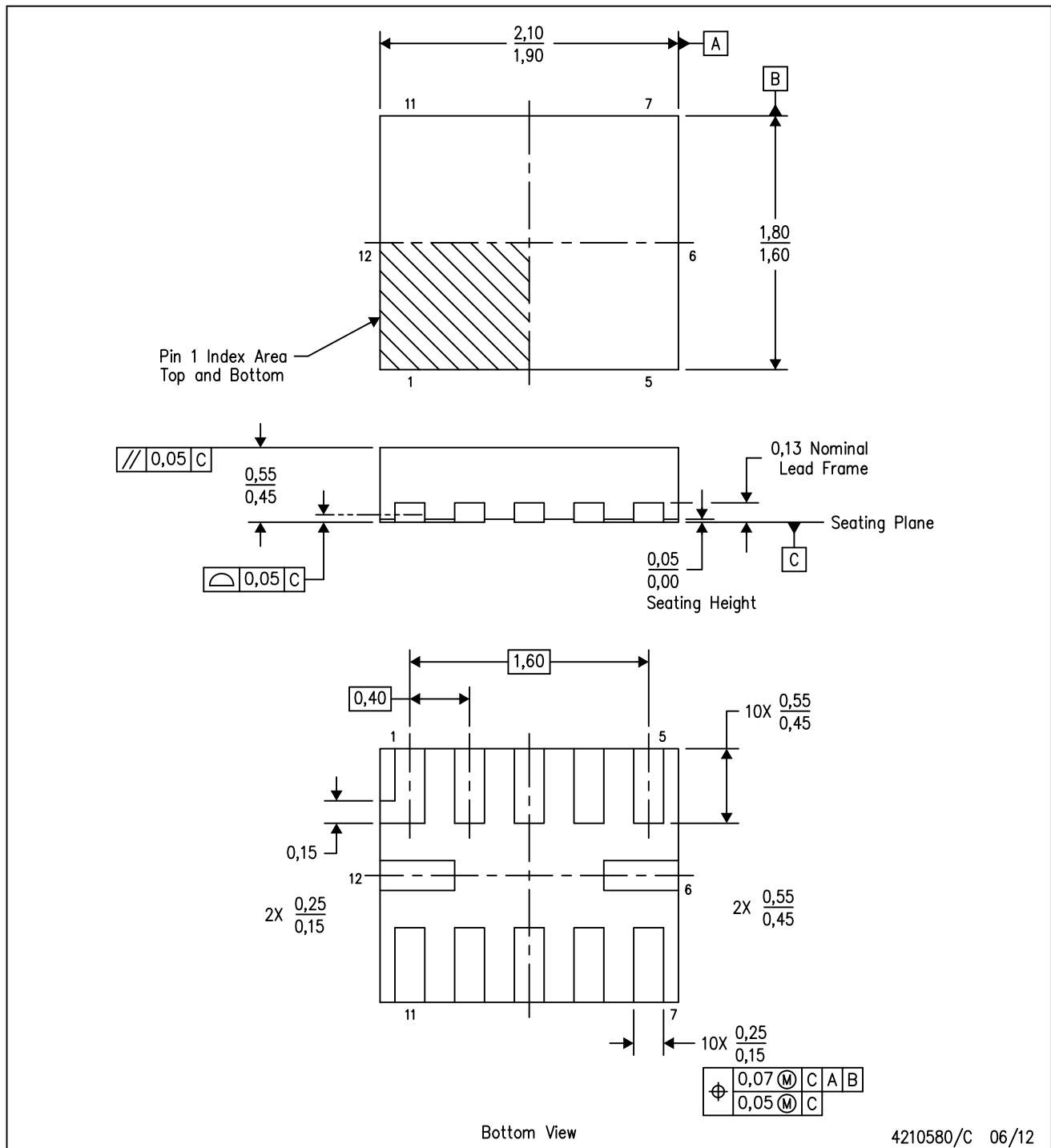
**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TXS4555RGTR	VQFN	RGT	16	3000	367.0	367.0	35.0
TXS4555RUTR	UQFN	RUT	12	3000	202.0	201.0	28.0

RUT (R-PUQFN-N12)

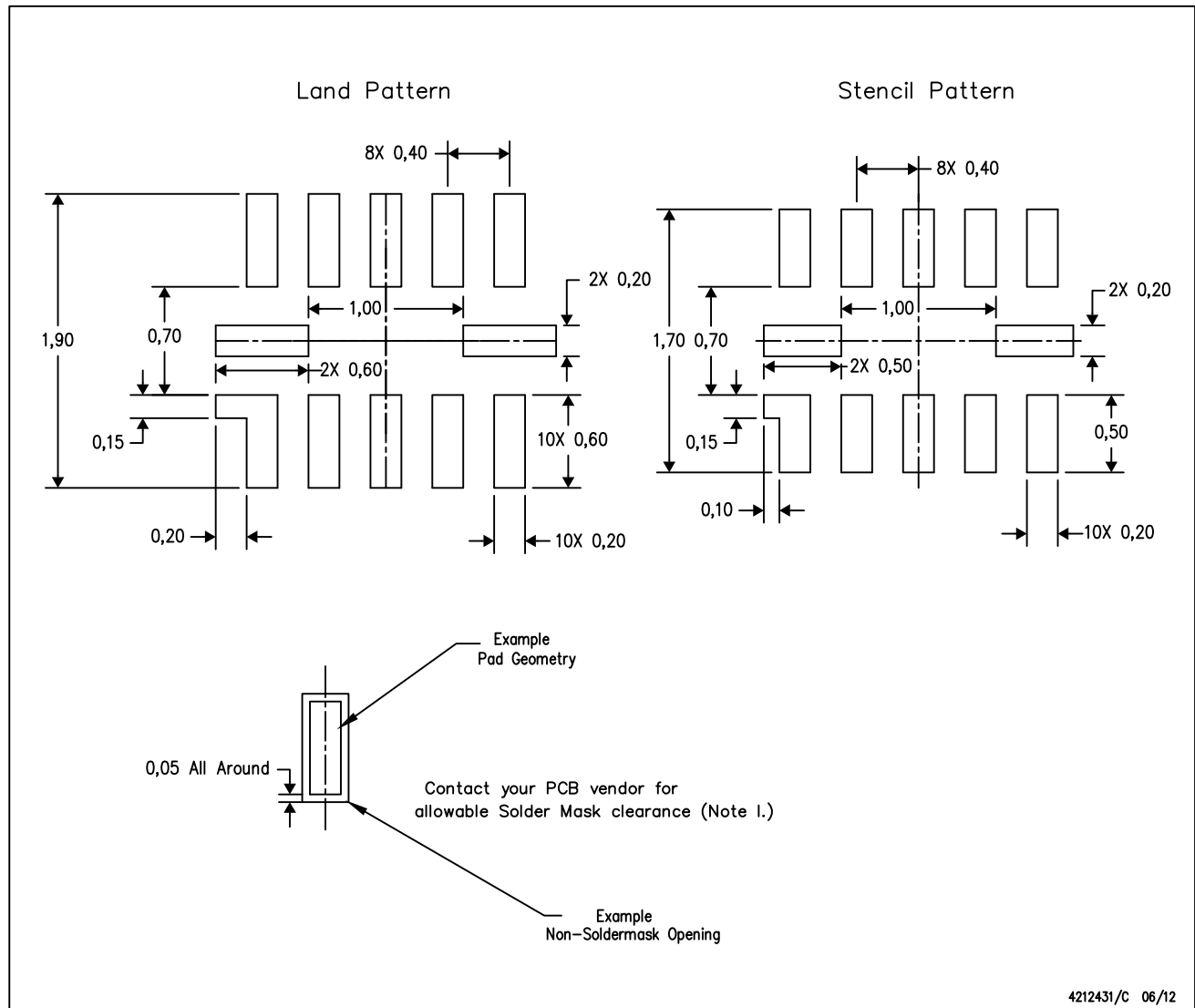
PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - QFN (Quad Flatpack No-Lead) package configuration.

RUT (R-PUQFN-N12)

PLASTIC QUAD FLATPACK NO-LEAD



4212431/C 06/12

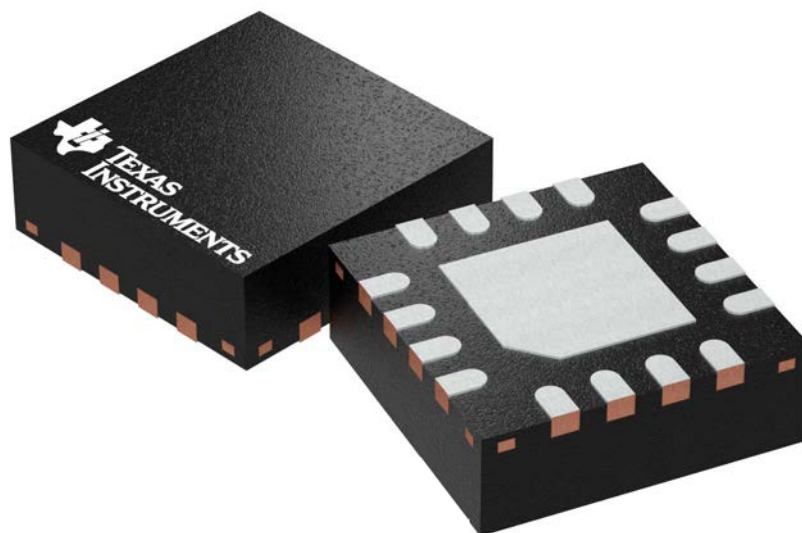
- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
  - E. Maximum stencil thickness 0,1016 mm (4 mils). All linear dimensions are in millimeters.
  - F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - G. Over-printing land for larger area ratio is not advised due to land width and bridging potential. Exercise extreme caution.
  - H. Suggest stencils cut with lasers such as Fiber Laser that produce the greatest positional accuracy.
  - I. Component placement force should be minimized to prevent excessive paste block deformation.

**RGT 16**

**GENERIC PACKAGE VIEW**

**VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD

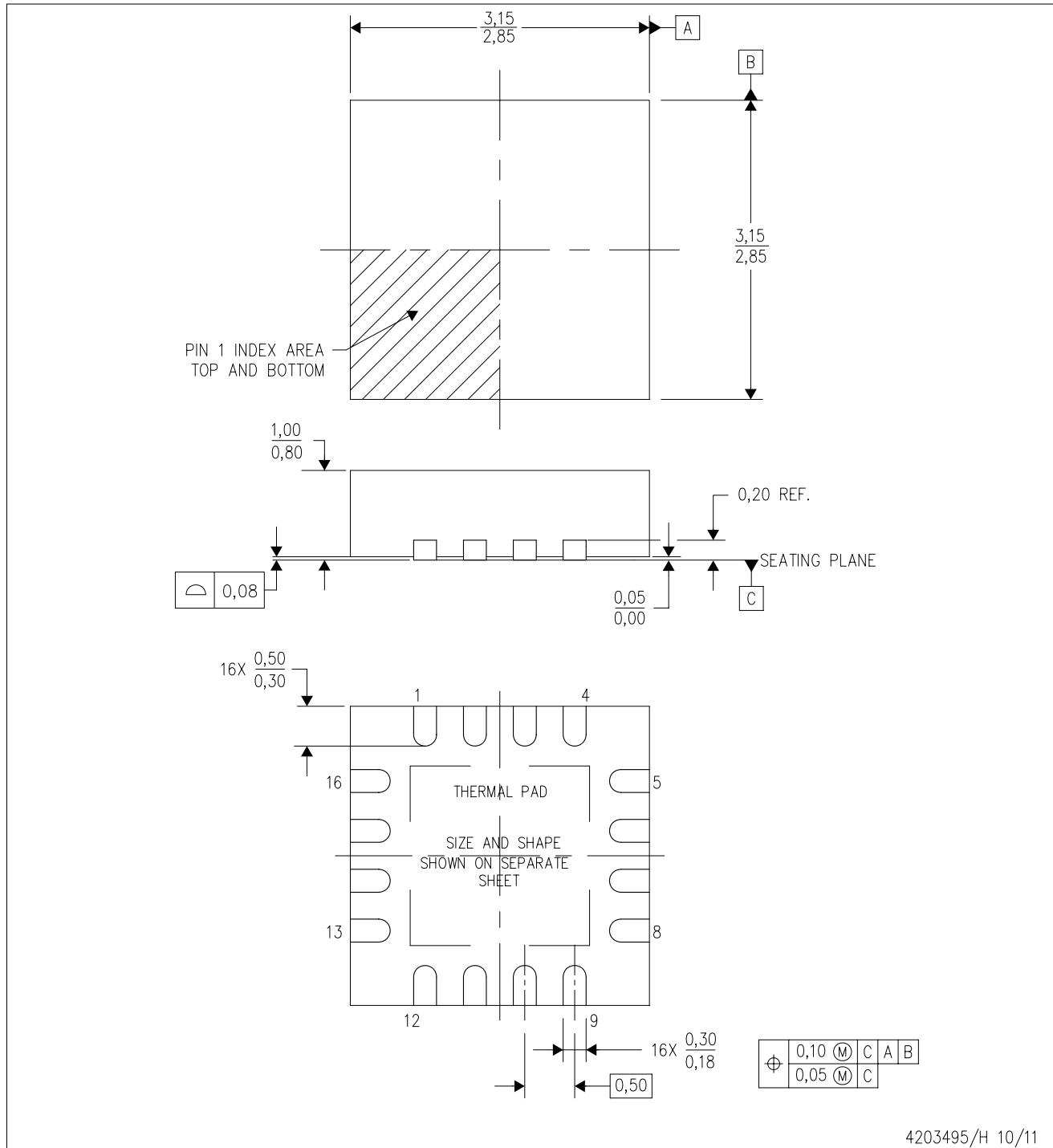


Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4203495/1

RGT (S-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



4203495/H 10/11

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - Quad Flatpack, No-leads (QFN) package configuration.
  - The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - Falls within JEDEC MO-220.

# THERMAL PAD MECHANICAL DATA

RGT (S-PVQFN-N16)

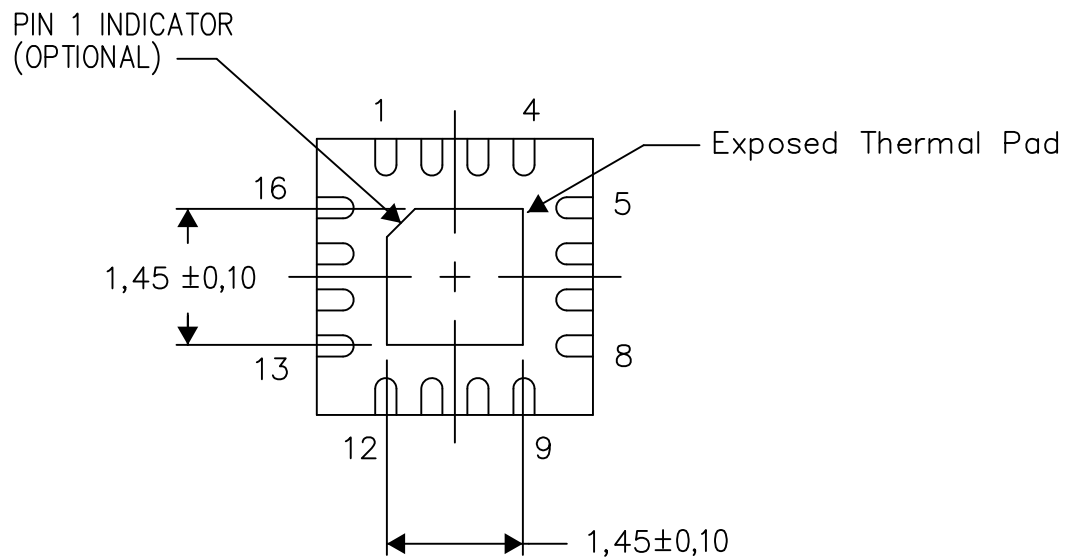
PLASTIC QUAD FLATPACK NO-LEAD

## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206349-2/Z 08/15

NOTE: All linear dimensions are in millimeters

## IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.