

Low Power Consumption Step-down DC/DC Controller IC

■ GENERAL DESCRIPTION

The XC9252 series is a 30V operation step-down DC/DC controller IC. The external P-ch driver transistor is used to achieve a stable operation under low input voltage. Low ESR capacitors such as ceramic capacitors can be used for the load capacitor (C_L).

A 0.8V reference voltage source is incorporated, and the output voltage can be set freely from 1.5V using external resistors (R_{FB1} , R_{FB2}).

280kHz to 550kHz can be selected for the switching frequency by connecting an external resistor to the R_{OSC} pin. The generation of unneeded noise can be reduced by this synchronization with an external CLK within $\pm 25\%$ of the internal clock using the MODE/SYNC pin. In automatic PWM/PFM control, the IC operates by PFM control when the load is light to achieve high efficiency over the full load range from light to heavy.

The soft start time can be set as desired by adding an external capacitance to the SS pin.

With the built-in UVLO function, the driver transistor is forced OFF when input voltage becomes 2.5V or lower.

Internal protection circuits include over current protection, short-circuit protection, and thermal shutdown circuits to enable safe use.

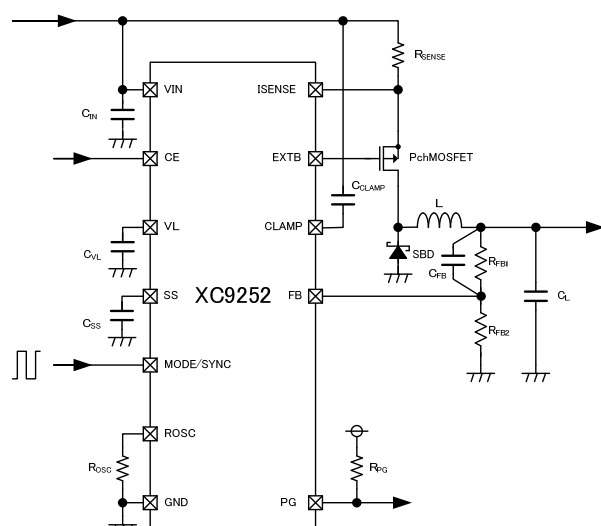
■ APPLICATIONS

- Car navigation systems
- Car audios
- ETC automotives

■ FEATURES

Input Voltage Range	: 3.0V~30V (Absolute MAX. Rating: 36V)
FB Voltage	: 0.8V ($\pm 2\%$)
Supply Current	: 30 μ A (@300kHz)
Oscillation Frequency	: 280kHz~550kHz (External Resistor)
External Clocking Synchronous	: $\pm 25\%$ of the internal clock
Control Method	: PWM control (MODE:H) PWM/PFM (MODE:L)
Soft-Start	: External set (External C)
Protection Circuits	: Over current limit (External Resistor) Automatic Return (XC9252A/B) Integral latch protection (XC9252C) Thermal shutdown
Output Capacitor	: Low ESR Capacitor
Operating Ambient Temperature	: $-40^{\circ}\text{C} \sim +105^{\circ}\text{C}$
Packages	: TSSOP-16 (XC9252A/C) USP-10B (XC9252B)
Environmentally Friendly	: EU RoHS Compliant, Pb Free

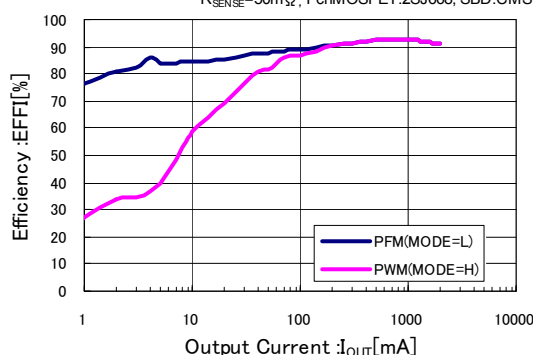
■ TYPICAL APPLICATION CIRCUIT



■ TYPICAL PERFORMANCE CHARACTERISTICS

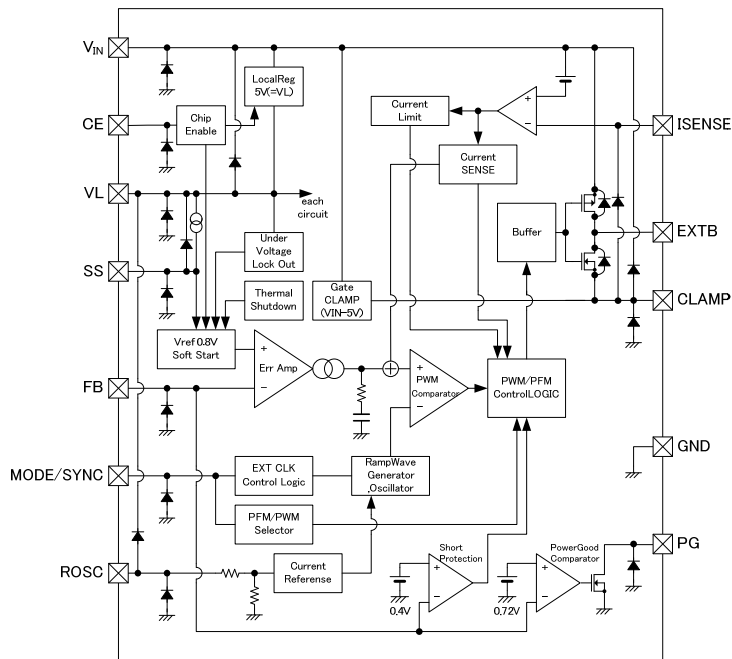
XC9252x08A ($V_{IN}=12\text{V}$, $V_{OUT}=5.7\text{V}$, $f_{OSC}=280\text{kHz}$)

$L=22\mu\text{H}$ (CLF12555-220M), $C_N=10\mu\text{F}$ (GRM32ER71H106KA12L),
 $R_{OSC}=300\text{k}\Omega$, $C_L=22\mu\text{F} \times 2$ (GRM32ER71E226KE15L),
 $R_{SENSE}=50\text{m}\Omega$, PchMOSFET: 2SJ668, SBD: CMS15

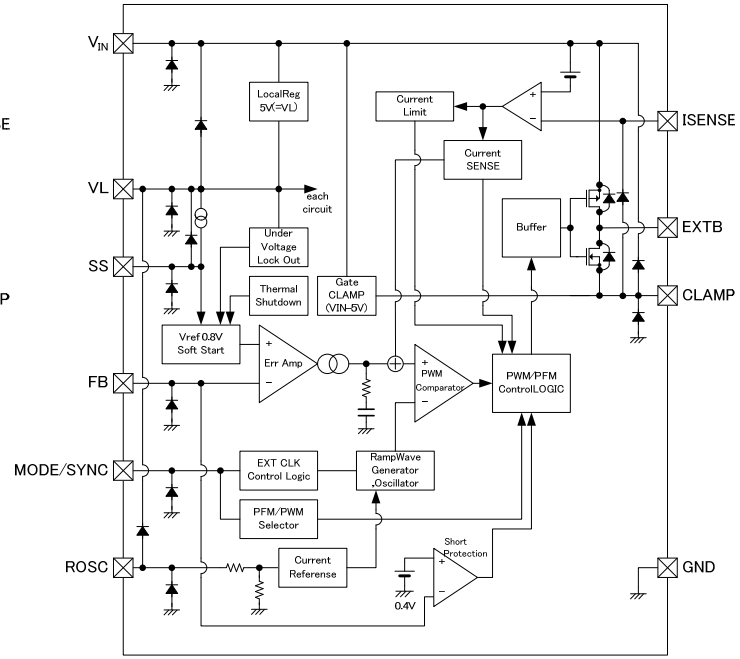


BLOCK DIAGRAM

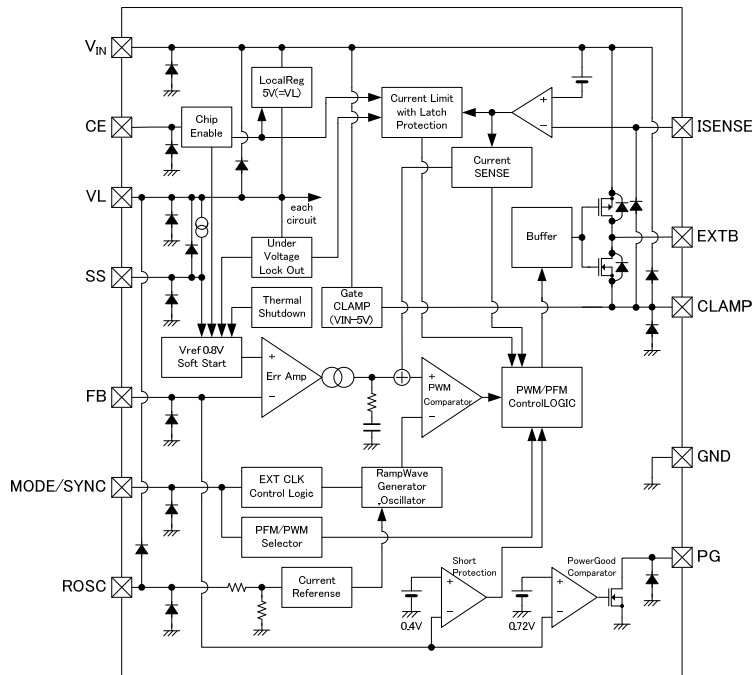
1) XC9252 Series, Type A



2) XC9252 Series, Type B



3) XC9252 Series, Type C



* Diodes inside the circuit are an ESD protection diode and a parasitic diode.

■PRODUCT CLASSIFICATION

●Ordering Information

XC9252①②③④⑤⑥-⑦

DESIGNATOR	ITEM	SYMBOL	DESCRIPTION
①	TYPE	A	Refer to Selection Guide
		B	
		C	
②③	Adjustable Output Voltage	08	Reference voltage is fixed in 0.8V
④	Oscillation Frequency	A	Adjustable
⑤⑥-⑦ (*1)	Packages (Order Unit)	VR-G	TSSOP-16 (3,000pcs/Reel) *Only Type A,C
		DR-G	USP-10B (3,000pcs/Reel) (*2) *Only Type B

(*1) The "-G" suffix denotes Halogen and Antimony free as well as being fully EU RoHS compliant.

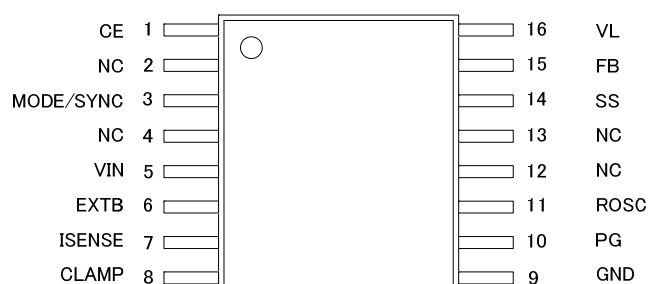
(*2) The USP-10B reels are shipped in a moisture-proof packing.

●Selection Guide

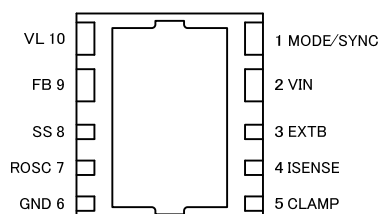
TYPE	CHIP ENABLE	SOFT-START	CURRENT LIMITER	LATCH PROTECTION	THERMAL SHUTDOWN	UVLO
A	Yes	Yes	Yes	No	Yes	Yes
B	No	Yes	Yes	No	Yes	Yes
C	Yes	Yes	Yes	Yes	Yes	Yes

TYPE	SYNCHRONIZED WITH EXTERNAL CLOCK	POWER-GOOD
A	Yes	Yes
B	Yes	No
C	Yes	Yes

■PIN CONFIGURATION



TSSOP-16
(TOP VIEW)



USP-10B
(BOTTOM VIEW)

* The dissipation pad for this IC should be solder-plated for mounting strength and heat dissipation. Please refer to the reference mount pattern and metal masking. The dissipation pad should be connected to the GND (No. 6) pin.

PIN ASSIGNMENT

PIN NUMBER		PIN NAME	FUNCTIONS
TSSOP-16	USP-10B		
5	2	VIN	Power Input
1	-	CE	Chip Enable
16	10	VL	Local Power Supply
10	-	PG	Power-good Output
14	8	SS	Soft-start Adjustment
15	9	FB	Output Voltage Sense
3	1	MODE/SYNC	Mode Control/External CLK Sync Pin
11	7	ROSC	Frequency Adjustment
9	6	GND	Ground
8	5	CLAMP	High Side Gate Clamp
7	4	ISENSE	Current Sense Pin
6	3	EXTB	External Transistor Drive Pin
2, 4, 12, 13	-	NC	No Connection

FUNCTION

XC9252 Series, Type A and Type C

PIN NAME	SIGNAL	STATUS
CE	L	Stand-by
	H	Active
	OPEN	Undefined State ^(*)

XC9252 Series

PIN NAME	SIGNAL	STATUS
MODE /SYNC	L	PWM/PFM Automatic Control
	H	PWM control
	CLK	Synchronized with External Clock Signal (PWM control)
	OPEN	Undefined State ^(*)

^(*) Please do not leave the CE and MODE/SYNC pin open.

■ABSOLUTE MAXIMUM RATINGS

Ta=25°C

PARAMETER		SYMBOL	RATINGS	UNITS
VIN Pin Voltage		VIN	-0.3 ~ +36	V
CE Pin Voltage		VCE	-0.3 ~ +36	V
FB Pin Voltage		VFB	-0.3 ~ +6.5	V
VL Pin Voltage		VVL	-0.3 ~ VIN+0.3 or +6.5 ^{(*)1}	V
VL Pin Current		IVL	10	mA
SS Pin Voltage		VSS	-0.3 ~ VVL+0.3 or +6.5 ^{(*)2}	V
ROSC Pin Voltage		VROSC	-0.3 ~ VVL+0.3 or +6.5 ^{(*)2}	V
MODE/SYNC Pin Voltage		VMODE	-0.3 ~ +6.5	V
PG Pin Voltage ^{(*)6}		VPG	-0.3 ~ +6.5	V
PG Pin Current ^{(*)6}		IPG	5	mA
CLAMP Pin Voltage		VCLAMP	-0.3 or VIN-6.5 ^{(*)4} ~ VIN+0.3 or +36 ^{(*)3}	V
CLAMP Pin Current		ICLAMP	10	mA
ISENSE Pin Voltage		VISENSE	-0.3 or VIN-6.5 or VCLAMP-0.3 ^{(*)5} ~ VIN+0.3 or +36 ^{(*)3}	V
EXTB Pin Voltage		VEXT	-0.3 or VIN-6.5 or VCLAMP-0.3 ^{(*)5} ~ VIN+0.3 or +36 ^{(*)3}	V
EXTB Pin Current		IEXT	100	mA
Power Dissipation	TSSOP-16	Pd	350	mW
	USP-10B		150	
Surge Voltage		VSURGE	46 ^{(*)7}	-
Operating Ambient Temperature		Topr	-40~+105	°C
Storage Temperature		Tstg	-55~+125	°C

* All voltages are described based on the GND pin.

^{(*)1} The maximum value should be either VIN+0.3 or +6.5 in the lowest.

^{(*)2} The maximum value should be either VVL+0.3 or +6.5 in the lowest.

^{(*)3} The maximum value should be either VIN+0.3 or +36 in the lowest.

^{(*)4} The minimum value should be either -0.3 or VIN-6.5 in the highest.

^{(*)5} The minimum value should be either -0.3 or VIN-6.5 or VCLAMP-0.3 in the highest.

^{(*)6} For the XC9252 Type A and C only.

^{(*)7} Applied Time ≤ 400ms

ELECTRICAL CHARACTERISTICS

XC9252 Series

Ta=25°C

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	CIRCUIT
FB Voltage	V _{FB}	-	0.784	0.800	0.816	V	②
Output Voltage Setting Range	V _{OUTSET}	-	1.5 ^(*)	-	V _{IN}	V	③
Operating Voltage Range	V _{IN}	-	3	-	30	V	-
Local Regulator Output Voltage	V _{VL}	I _{VL} =0.1mA	4.75	5.00	5.25	V	②
Gate Clamp Voltage	V _{CLAMP}	I _{CLAMP} =0.1mA, V _{CLAMP} =V _{IN} -CLAMP	4.75	5.00	5.25	V	②
UVLO Detect Voltage	V _{UVLO1}	V _{IN} : 2.8V→2.3V, V _{CE} =12V, V _{FB} =0.72V V _{IN} Voltage when EXT _B pin voltage changes from "L" level to "H" level	2.375	2.500	2.625	V	②
UVLO Release Voltage	V _{UVLO2}	V _{IN} : 2.3V→2.8V, V _{CE} =12V, V _{FB} =0.72V V _{IN} Voltage which EXT _B pin voltage changes from "H" level to "L" level	2.470	2.600	2.730	V	②
UVLO Detect Time	t _{UVLO}	V _{IN} : 2.8V→2.3V, V _{CE} =12V, V _{FB} =0.72V V _{IN} Voltage when EXT _B pin voltage changes from "L" level to "H" level	0.20	0.35	0.60	ms	②
Supply Current	I _{DD}	V _{IN} =V _{CE} =30V, V _{MODE} =5V, V _{FB} =0.95V(PWM)	70	95	120	μA	①
Quiescent Current 1	I _{q1}	V _{IN} =V _{CE} =30V, V _{MODE} =0V, V _{FB} =0.95V (PWM/PFM) R _{OSC} =270kΩ	18	30	46	μA	①
Quiescent Current 2	I _{q2}	V _{IN} =V _{CE} =30V, V _{MODE} =0V, V _{FB} =0.95V (PWM/PFM)	25	36	55	μA	①
Stand-by Current	I _{STB}	V _{IN} =30V, V _{CE} =0V	-	0	1	μA	①
Operating Oscillation Frequency Setting Range	f _{OSCSET}	-	280	-	550	kHz	③
Oscillation Frequency 1	f _{OSC1}	Connected to external components, I _{OUT} =100mA, R _{OSC} : 270kΩ, L=22 μH	270	300	330	kHz	③
Oscillation Frequency 2	f _{OSC2}	Connected to external components, I _{OUT} =100mA	414	460	506	kHz	③
External Clock Signal Synchronized Frequency	SYNCOSC	Connected to external components, V _{IN} =V _{CE} =12V, I _{OUT} =100mA	f _{OSC} ×0.75	f _{OSC}	f _{OSC} ×1.25	kHz	③
External Clock Signal Duty Cycle	D _{SYNC}	Connected to external components	25	-	75	%	③
Maximum Duty Cycle	D _{MAX}	V _{FB} =0.65V	100	-	-	%	②
Minimum Duty Cycle	D _{MIN}	V _{FB} =0.95V	-	-	0	%	②
EXT _B "H" SW On Resistance	R _{EXTH}	V _{IN} =V _{CE} =5V, V _{CLAMP} =0V, V _{FB} =0.95V, I _{EXT} =50mA	2.0	3.5	6.0	Ω	②
EXT _B "L" SW On Resistance	R _{EXTL}	V _{IN} =V _{CE} =5V, V _{CLAMP} =0V, V _{FB} =0.65V, I _{EXT} =-50mA	1.4	2.5	6.0	Ω	②
Current Limit Voltage 1 ^(*)	V _{ISENSE1}	V _{ISENSE} =V _{IN} →V _{IN} -0.20V, V _{FB} =0.65V, R _{OSC} : 270kΩ V _{ISENSE} Voltage when EXT _B pin voltage changes from "L" level to "H" level	127.5	150	172.5	mV	②
Current Limit Voltage 2 ^(*)	V _{ISENSE2}	V _{ISENSE} =V _{IN} →V _{IN} -0.15V, V _{FB} =0.65V V _{ISENSE} Voltage when EXT _B pin voltage changes from "L" level to "H" level	85	100	115	mV	②
Latch Time1 ^(*)	t _{LAT1}	V _{ISENSE} =V _{IN} →V _{IN} -0.2V, V _{FB} =0.65V, R _{OSC} : 270kΩ V _{ISENSE} Voltage when EXT _B pin voltage changes from "L" level to "H" level	1.2	1.9	2.3	ms	③
Latch Time2 ^(*)	t _{LAT2}	V _{ISENSE} =V _{IN} →V _{IN} -0.2V, V _{FB} =0.65V V _{ISENSE} Voltage when EXT _B pin voltage changes from "L" level to "H" level	0.8	1.2	1.5	ms	③
Short Protection Threshold Voltage ^(*)	V _{SHORT}	V _{FB} =0.5V→0.3V, V _{FB} Voltage when Oscillation Frequency is decreased	0.35	0.40	0.45	V	③
Internal Soft-start Time	t _{SS1}	V _{CE} =0→12V, V _{SS} =5V, V _{FB} =V _{FB} ×0.9V Time until EXT _B pin oscillates	0.5	0.8	1.2	ms	②
External Soft-start Time	t _{SS2}	V _{CE} =0→12V, V _{FB} =V _{FB} ×0.9V, C _{SS} =4700pF Time until EXT _B pin oscillates	4.0	5.6	7.0	ms	②

NOTE:

Unless otherwise stated, V_{IN}=V_{CE}=12V, SS:OPEN, R_{OSC}:160kΩ, C_{VL}=1 μF, C_{CLAMP}=1 μF

External Components: L=10 μH, C_{IN}=10 μF, C_L=22 μF, R_{SENSE}=33mΩ, R_{FB1}=220kΩ, R_{FB2}=36kΩ, C_{FB}=33pF (V_{OUTSET}=5.7V)

(*) Please use within the range of V_{OUT}/V_{IN}≥0.15

(*) Current limit denotes the level of detection at peak of coil current.

(*) EFFI = { (output voltage × output current) / (input voltage × input current) } × 100

(*) For the XC9252 Type C only

(*) For the XC9252 Type A and B only

(*) For the XC9252 Type A and C only

■ ELECTRICAL CHARACTERISTICS (Continued)

XC9252 Series

Ta=25°C

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	CIRCUIT
SS Pin Current 1	I _{SS1}	V _{FB} =0.95V, V _{SS} =0V, R _{OSC} : 270kΩ	0.6	0.8	1.2	μA	②
SS Pin Current 2	I _{SS2}	V _{FB} =0.95V, V _{SS} =0V	1.4	1.7	2.0	μA	②
Efficiency ^{(*)3}	EFFI	Connected to external components, V _{OUT} =5.7V, I _{OUT} =1A	-	90	-	%	③
FB Voltage Temperature Characteristics	$\frac{\Delta V_{FB}}{(\Delta T_{opr} \cdot V_{FB})}$	I _{OUT} =100mA, -40°C ≤ T _{opr} ≤ 105°C	-	±50	-	ppm/°C	②
PG detect voltage ^{(*)6}	V _{PG}	V _{FB} =0.76V→0.65V, R _{PG} : 200kΩ pull-up to VL Voltage when PG pin voltage changes from "H" level to "L" level	0.691	0.720	0.749	V	②
PG Output Current ^{(*)6}	I _{PG}	V _{FB} =0.65V, V _{PG} =0.5V	1	-	-	mA	②
MODE/SYNC 'H' Voltage	V _{MODEH}	-	1.2	-	6.0	V	③
MODE/SYNC 'L' Voltage	V _{MODEL}	-	GND	-	0.45	V	③
MODE/SYNC 'H' Current	I _{MODEH}	V _L =V _{MODE} =6V	-0.1	0	0.1	μA	①
MODE/SYNC 'L' Current	I _{MODEL}	V _L =6V, V _{MODE} =0V	-0.1	0	0.1	μA	①
FB 'H' Current	I _{FBH}	V _{SYNC} =0V, V _{FB} =6V	-0.1	0	0.1	μA	①
FB 'L' Current	I _{FBL}	V _{SYNC} =0V, V _{FB} =0V	-0.1	0	0.1	μA	①
CE 'H' Voltage ^{(*)6}	V _{CEH}	V _{CE} =0.7→2.8V, V _{IN} =30V, V _{MODE} =0V, V _{FB} =0.65V Voltage when EXT _B pin voltage changes from "H" level to "L" level	2.8	-	30	V	②
CE 'L' Voltage ^{(*)6}	V _{CEL}	V _{CE} =2.8→0.7V, V _{IN} =30V, V _{MODE} =0V, V _{FB} =0.65V Voltage when EXT _B pin voltage changes from "L" level to "H" level	GND	-	0.7	V	②
CE 'H' Current ^{(*)6}	I _{CEH}	V _{IN} =V _{CE} =30V, V _{MODE} =0V	-0.1	0	0.1	μA	①
CE 'L' Current ^{(*)6}	I _{CEL}	V _{IN} =30V, V _{CE} =V _{MODE} =0V	-0.1	0	0.1	μA	①
Thermal Shutdown Temperature	T _{TSD}	Junction Temperature	-	150	-	°C	②
Hysteresis Width	T _{HYS}	Junction Temperature	-	25	-	°C	②

NOTE:

Unless otherwise stated, V_{IN}=V_{CE}=12V, SS:OPEN, R_{OSC}:160kΩ, C_{VL}=1 μF, C_{CLAMP}=1 μF

External Components: L=10 μH, C_{IN}=10 μF, C_L=22 μF, R_{SENSE}=33mΩ, R_{FB1}=220kΩ, R_{FB2}=36kΩ, C_{FB}=33pF (V_{OUTSET}=5.7V)

^{(*)3} EFFI = { (output voltage × output current) / (input voltage × input current) } × 100

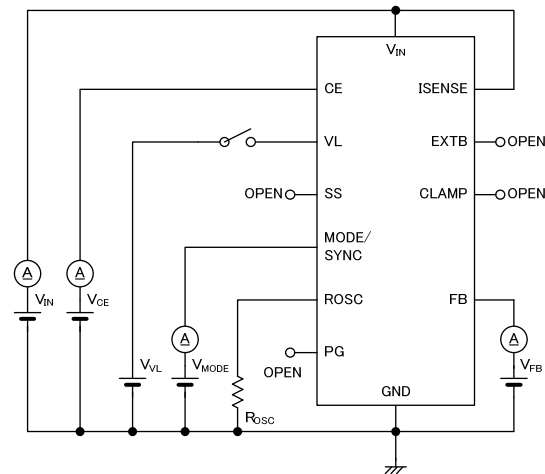
^{(*)4} For the XC9252 Type C only

^{(*)5} For the XC9252 Type A and B only

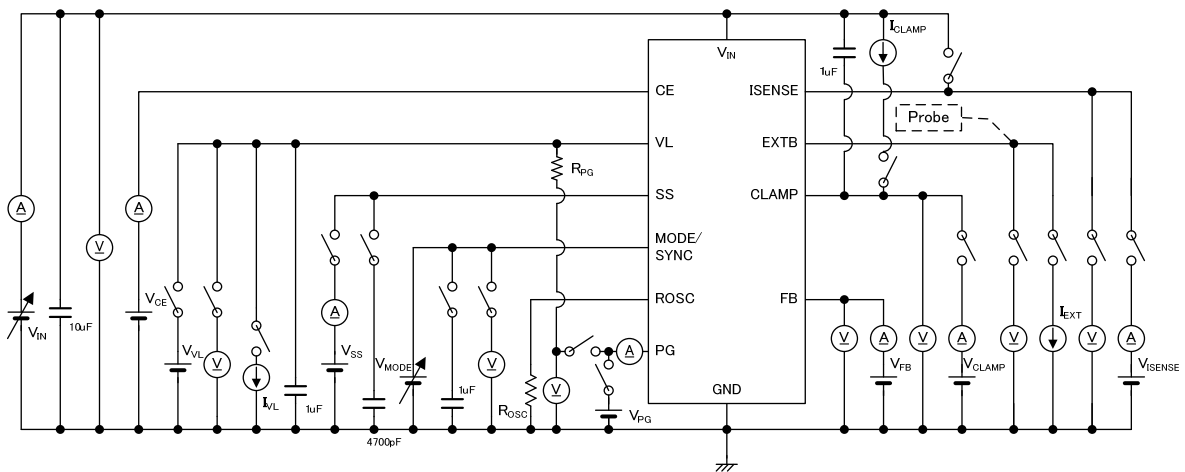
^{(*)6} For the XC9252 Type A and C only

TEST CIRCUITS

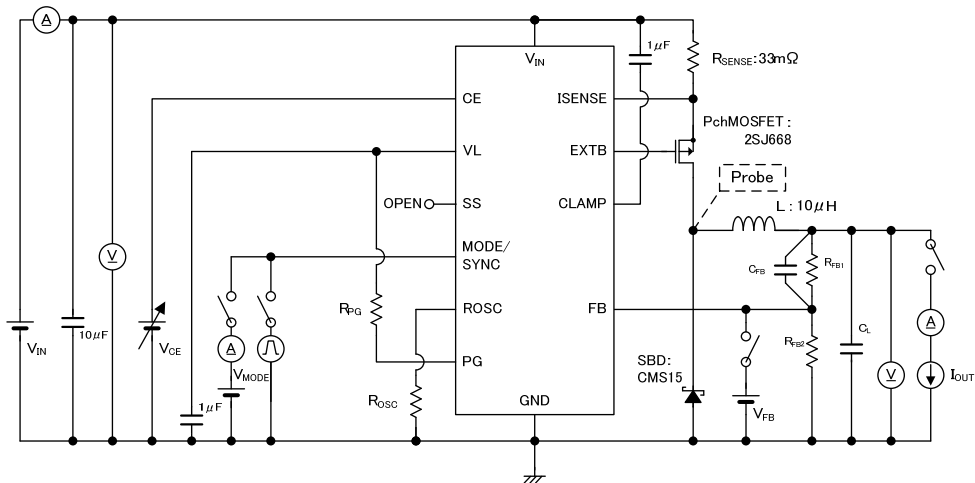
CIRCUIT①



CIRCUIT②

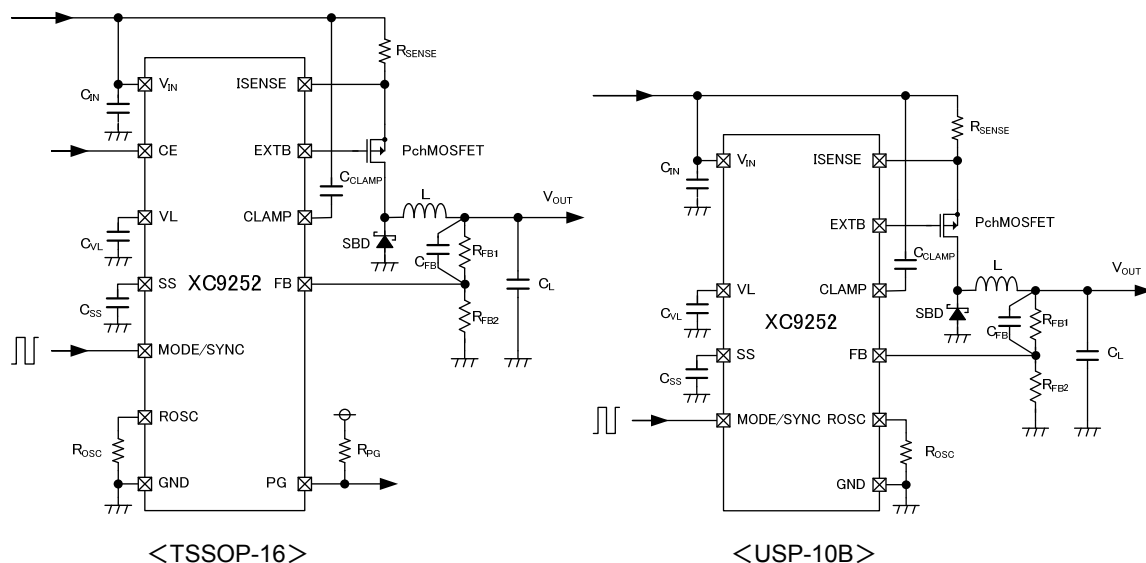


CIRCUIT③



(*) The Type B does not have the CE and PG pin.

■ TYPICAL APPLICATION CIRCUIT



【Typical Examples】

	MANUFACTURER	PRODUCT NUMBER	VALUE
L	TDK	CLF10040T-4R7M	4.7 μ H
		CLF10040T-100M	10 μ H
		CLF12555T-220M	22 μ H
Pch MOSFET	TOSHIBA	2SJ668	$V_{DS}=60V/I_{DS}=5A/R_{ON}=250m\Omega$
	SANYO	CPH3351	$V_{DS}=60V/I_{DS}=1.8A/R_{ON}=330m\Omega$
SBD	TOSHIBA	CMS15	$V_F=0.58V(3A)$
		CLS03	$V_F=0.58V(10A)$
C_{IN}	Murata	GRM32ER71H106K	10 μ F/50V
C_L	Murata	GRM32ER71E226K	22 μ F/25V
	Panasonic	20SVP22M	22 μ F/20V/ESR=60m Ω
	Panasonic	20SVP47M	47 μ F/20V/ESR=45m Ω
C_{VL}, C_{CLAMP}	Murata	GRM188R71A105K	1 μ F/10V

<Output voltage setting>

The output voltage can be set by adding an external dividing resistor. The output voltage is determined by the equation below based on the values of R_{FB1} and R_{FB2} .

$$V_{OUT} = 0.8 \times (R_{FB1} + R_{FB2}) / R_{FB2}$$

with $R_{FB1} + R_{FB2} \leq 1M\Omega$

Adjust the value of the phase compensation speed-up capacitor C_{FB} using the equation below.

$$C_{FB} = \frac{1}{2\pi \times f_{zfb} \times R_{FB1}}$$

A target value for f_{zfb} of about $\frac{2}{2\pi \sqrt{C_L \times L}}$ is optimum.

【Setting Example】

When $R_{FB1}=220k\Omega$, $R_{FB2}=36k\Omega$, $V_{OUT}=0.8 \times (220k\Omega + 36k\Omega) / 36k\Omega = 5.69V$

When $C_L=22\mu F$, $L=10\mu H$, and f_{zfb} is set to a target of 21.46kHz using the above equation,

$C_{FB}=1/(2 \times \pi \times 21.46kHz \times 220k\Omega)=33pF$

* The setting range for the output voltage is 1.5V to V_{IN} . The condition $V_{OUT}/V_{IN} \geq 0.15$ must be satisfied.

■ TYPICAL APPLICATION CIRCUIT (Continued)

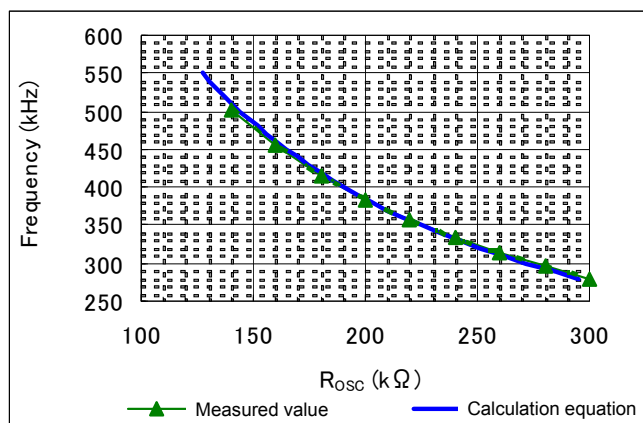
<Switching frequency setting>

In the XC9252 series, the switching frequency can be set to any value in the range 280kHz to 550kHz by connecting a resistance (R_{OSC}) between the R_{OSC} pin and GND. R_{OSC} is determined by the equation below.

$$R_{OSC} = (30 \times f_{OSCSET} - 83016) / (27.4 - f_{OSCSET})$$

R_{OSC} : Switching frequency setting resistance [k Ω]

f_{OSCSET} : Set frequency [kHz]



【Setting Example】

Switching Frequency	R_{OSC}
300kHz	270k Ω
460kHz	160k Ω

<Inductance value setting>

In the XC9252 series, it is optimum to set an inductance value within the range below based on the switching frequency.

Switching Frequency	L
280kHz $\leq f_{OSCSET} < 400$ kHz	10 μ H ~ 22 μ H
400kHz $\leq f_{OSCSET} \leq 550$ kHz	4.7 μ H ~ 10 μ H

< C_L setting >

In the XC9252 series, a low ESR capacitor can be used for the load capacitance C_L ; however, if a ceramic capacitor is used, the set voltage is restricted to 2.5V or higher. If less than 2.5V, an OS-CON (conductive polymer aluminum solid electrolytic capacitor) is recommended. Select according to the set voltage and switching frequency as shown in the table below. Select a capacitor with good temperature characteristics and bias dependence characteristics.

Switching Frequency	$V_{OUTSET} < 2.5V$	$V_{OUTSET} \geq 2.5V$
	OS-CON	Ceramic
280kHz $\leq f_{OSCSET} < 400$ kHz	47 μ F	22 μ F $\times 2$
400kHz $\leq f_{OSCSET} \leq 550$ kHz	22 μ F	22 μ F

■ TYPICAL APPLICATION CIRCUIT (Continued)

<Limit current setting>

In the XC9252 series, a resistance can be connected between the V_{IN} pin and I_{SENSE} pin to set a limit current. The sense resistance (R_{SENSE}) is determined by the equation below.

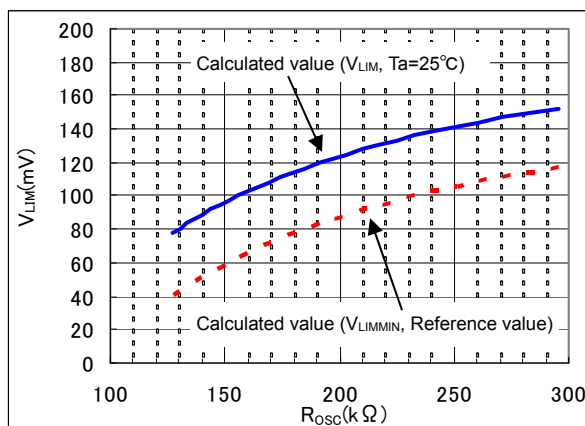
$$R_{SENSE} = V_{LIM} / I_{LIM}$$

I_{LIM} : Limit current (peak current) [A]

R_{SENSE} : Sense resistance [$m\Omega$]

$V_{LIM} = (230 - (0.2765 \times f_{OSCSET}))$: Limit current detection voltage [mV]

f_{OSCSET} : Set frequency [kHz]



* The limit current detection voltage V_{LIM} varies depending on the temperature. Set the limit current (reference value) using the lower limit value given by the equation below.

$$V_{LIMMIN} = (230 - (0.33 \times f_{OSCSET})) \times 0.85$$

V_{LIMMIN} : Lower limit value within operating temperature range (-40 to 105°C)

$$I_{LIMMIN} = V_{LIMMIN} / R_{SENSE} \text{ [A]}$$

【Calculation Example】

To set I_{LIM} to 3A with $f_{OSCSET}=460\text{kHz}$

$$R_{SENSE} = (230 - (0.2765 \times 460)) / 3 \div 34 \text{ [m}\Omega\text{]}$$

In this case, the lower limit value of the limit current is $I_{LIMMIN} = (230 - (0.33 \times 460)) \times 0.85 / 34 = 1.95 \text{ [A]}$

<Soft-start function>

The soft-start time of the XC9252 series can be adjusted externally (SS pin). The soft-start time is the time from the start of V_{CE} until the output voltage reaches 90% of the set voltage. The soft-start time depends on the external capacitance C_{SS} , and is determined by the equation below.

$$t_{SS2} = 0.002 \times C_{SS} / I_{SS} \text{ [ms]}$$

C_{SS} : External capacitance [pF]

$I_{SS} = f_{OSCSET} / 300 \text{ [}\mu\text{A, TYP.]}$

f_{OSCSET} : Set frequency [kHz]

* Note that the value of the soft-start time t_{SS2} varies depending on the effective capacitance value of the delay capacitance C_{SS} .

【Calculation Example】

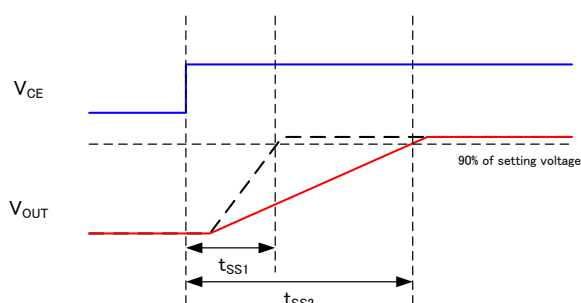
When $f_{OSCSET}=460\text{kHz}$, $C_{SS}=4700\text{pF}$

$$t_{SS2} = 0.002 \times 4700 / (460 / 300) = 6.13\text{ms}$$

The minimum value t_{SS1} of the soft-start time is set internally to about 0.8ms @460kHz (TYP.). The internal soft-start time is determined by the equation below.

$$t_{SS1} = 368 / f_{OSCSET} \text{ [ms]}$$

f_{OSCSET} : Set frequency [kHz]

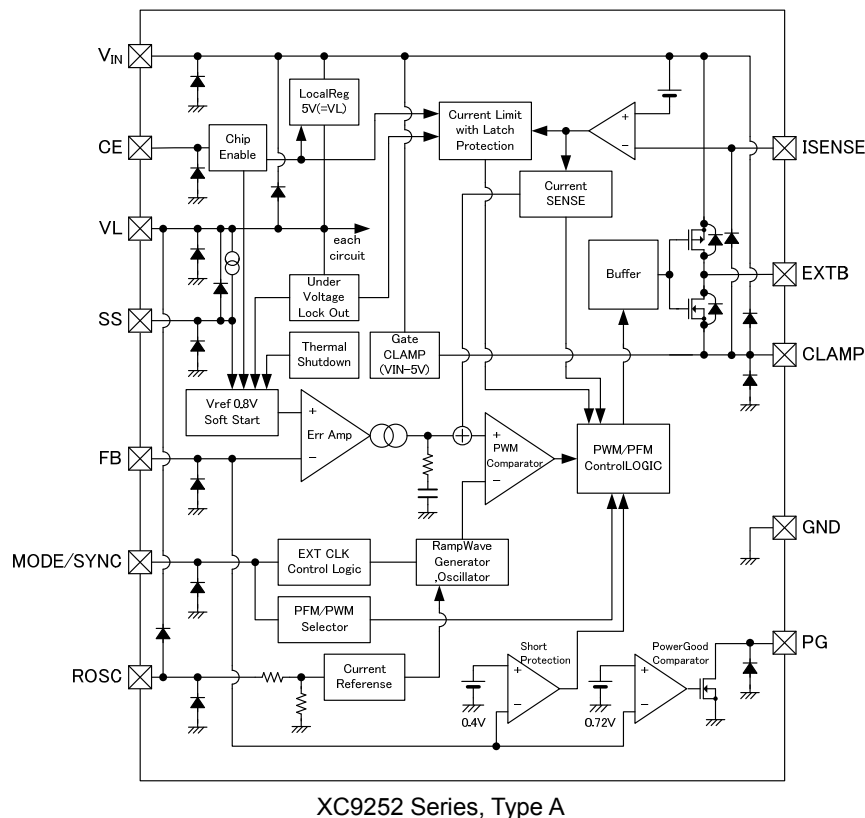


OPERATIONAL EXPLANATION

The XC9252 series consists internally of a reference voltage supply, ramp wave circuit, error amp, PWM comparator, phase compensation circuit, current limiting circuit, under-voltage lockout (UVLO) circuit, internal power supply (VL) circuit, gate clamp (CLAMP) circuit, thermal shutdown (TSD) circuit, oscillator (OSC) circuit, soft-start circuit, control block and other elements.

The voltage feed back from the FB pin is compared to the internal reference voltage by the error amp, the output from the error amp is phase compensated, and the signal is input to the PWM comparator to determine the ON time of switching during PWM operation. The output signal from the error amp is compared to the ramp wave by the PWM comparator, and the output is sent to the buffer drive circuit and output from the EXTB pin as the duty width of switching. This operation is performed continuously to stabilize the output voltage.

The driver transistor current is monitored at each switching by the ISENSE pin, and the output signal from the error amp is modulated as a multi-feedback signal. This allows a stable feedback system to be obtained even when a low ESR capacitor such as a ceramic capacitor is used, and this stabilizes the output voltage.



XC9252 Series, Type A

<Reference voltage source>

The reference voltage source provides the reference voltage to ensure stable output voltage of the DC/DC converter.

<Oscillator circuit>

The ramp wave circuit determines switching frequency. By connecting an external resistance R_{OSC} , operation at any switching frequency from 280kHz to 550kHz is possible.

Clock pulses generated in this circuit are used to produce ramp waveforms needed for PWM operation.

<Error amplifier>

The error amplifier is designed to monitor output voltage. The amplifier compares the reference voltage with the feedback voltage divided by the internal split resistors, R_{FB1} and R_{FB2} . When a voltage is lower than the reference voltage, then the voltage is fed back, the output voltage of the error amplifier increases. The error amplifier output is fixed internally to deliver an optimized signal to the mixer.

<Chip enable>

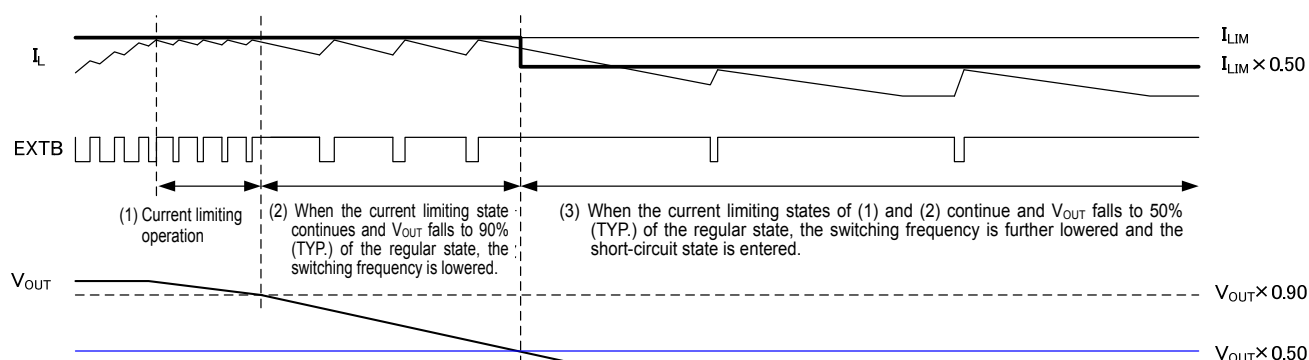
Types A and C can be put in the standby state by inputting L level into the CE pin. In the standby state, the quiescent current of the IC is $0\mu A$ (TYP.). When H level is input into CE pin, operation starts. The input of the CE pin is CMOS input and the sink current is $0\mu A$ (TYP.).

■ OPERATIONAL EXPLANATION (Continued)

<Current limiting, short-circuit protection>

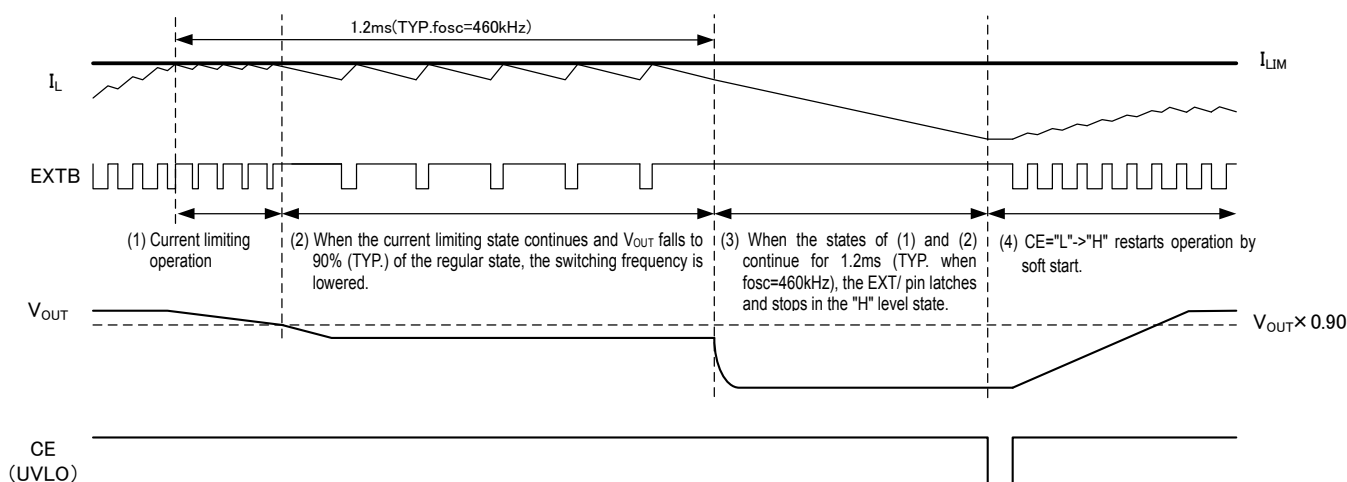
The current limiting circuits of types A and B combine both current limiting and short-circuit protection.

- (1) The current in the sense resistance (R_{SENSE}) connected to the V_{IN} pin - I_{SENSE} pin is monitored, and when the load current attains the limiting current, the current limiting circuit activates and the output voltage drops.
- (2) The output voltage drops to about 90% of the regular state, and this causes the switching frequency to drop and prevent coil current (I_L) overlay. When the limiter state is released and the output voltage returns to the regular state, the switching frequency returns to the frequency set by R_{OSC} .
- (3) If the output voltage drops further from states (2), the output current is limited, the switching frequency is lowered further, and the short-circuit state is entered. When the load becomes lighter than the short-circuit state, restart takes place automatically. To prevent overshoot during restart, restart takes place by soft-start.



<Integral latch protection>

When the current limiting state continues for a certain time, the correct limiting circuit of type C latches and stops the EXT/ pin in the "H" level state (turning off the driver T_r). To restart operation by soft-start once in the latch stop state, "L" level must be input into the CE pin followed by "H" level, or restart of the V_{IN} pin (briefly lowering the V_{IN} voltage below the UVLO detection voltage) must be performed.



<Thermal shutdown>

The thermal shutdown (TSD) as an over current limit is built in the XC9252 series.

When the junction temperature of the IC reaches the detection temperature, EXT_B becomes "H" level and forcibly stops output. When the junction temperature falls to the release temperature while in the output stop state, restart takes place by soft-start.

<UVLO>

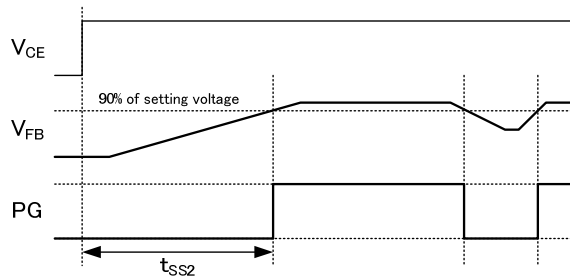
When the V_{IN} pin voltage falls below 2.5V (TYP.), EXT_B becomes "H" level and forcibly stops output to prevent false pulse output due to instable operation of the internal circuits. When the V_{IN} pin voltage rises above 2.6V (TYP.), the UVLO function is released, the soft-start function activates, and output start operation begins. Stopping by UVLO is not shutdown; only pulse output is stopped and the internal circuits continue to operate.

■ OPERATIONAL EXPLANATION (Continued)

<Power good>

On types A and C, the output state can be monitored using the power good function. When the FB voltage drops below 90% (TYP.), the PG pin outputs an "L" signal.

The PG pin is an Nch open drain output, therefore a pull-up resistance must be connected to the PG pin.

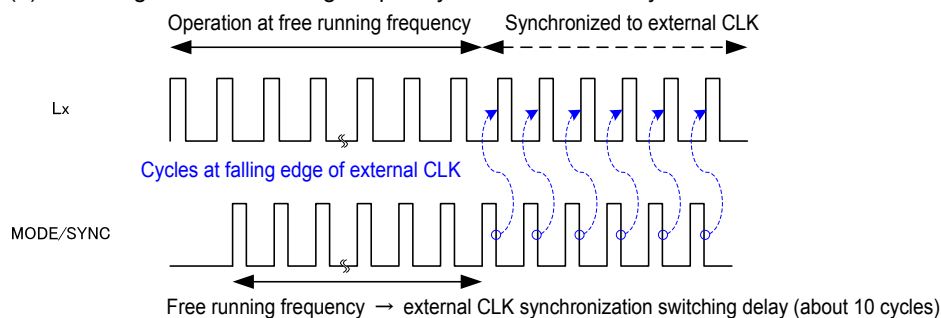


<SYNC/MODE function>

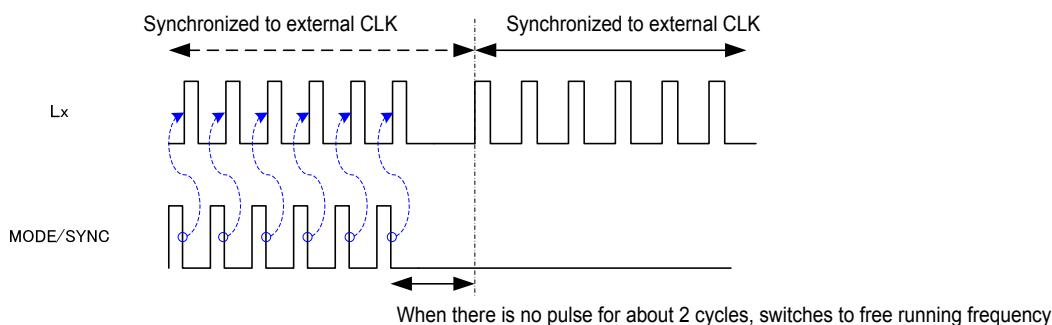
The MODE/SYNC pin has the two functions of a control MODE selector pin and an external CLK input pin. When "H" voltage is input, the mode becomes fixed PWM control, and when "L" voltage is input, the mode becomes PWM/PFM auto switching control.

When an external CLK ($\pm 25\%$ of free running frequency, on duty 25% to 75%) is input into the MODE/SYNC pin, operation is synchronized to the falling edge of the external CLK (external CLK synchronization function). When synchronized to the external CLK, the control mode is automatically PWM control. When the external CLK is fixed at "H" voltage or "L" voltage for about 2 cycles of the free running frequency, external CLK synchronization stops and operation at the free running frequency takes place.

(1) Switching from free running frequency => external CLK synchronization



(2) Switching from external CLK synchronization => free running frequency



■NOTE ON USE

1. For the phenomenon of temporal and transitional voltage decrease or voltage increase, the IC may be damaged or deteriorated if IC is used beyond the absolute MAX. specifications.
2. Make sure that the absolute maximum ratings of the external components and of this IC are not exceeded.
3. The DC/DC converter characteristics depend greatly on the externally connected components as well as on the characteristics of this IC, so refer to the specifications and standard circuit examples of each component when carefully considering which components to select. Be especially careful of the capacitor characteristics and use B characteristics (JIS standard) or X7R, X5R (EIA standard) ceramic capacitors.
4. If there is a large dropout voltage, then there might be pulse-skip during light loads even with PWM control.

5. The DC/DC converter of this IC uses a current-limiting circuit to monitor the coil peak current. If the potential dropout voltage is large or the load current is large, the peak current will increase, which makes it easier for current limitation to be applied which in turn could cause the operation to become unstable. When the peak current becomes large, adjust the coil inductance and sufficiently check the operation. The following formula is used to show the peak current.

$$\text{Peak Current: } I_{pk} = (V_{IN} - V_{OUT}) \times \text{OnDuty} / (2 \times L \times f_{osc}) + I_{OUT}$$

L: Coil Inductance [H]

f_{osc}: Oscillation Frequency [Hz]

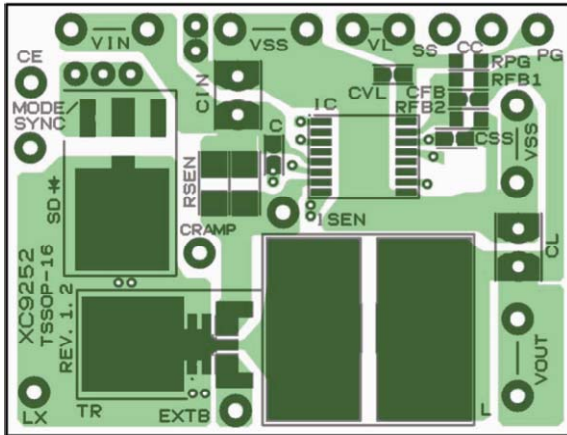
I_{OUT}: Load Current [A]

6. If there is a large dropout voltage, a circuit delay could create the ramp-up of coil current with staircase waveform exceeding the current limit.
7. The ripple voltage could be increased when switching from discontinuous conduction mode to Continuous conduction mode. Please apply the ICs only after careful examination by the customer.
8. When operation changes from free running frequency to external CLK synchronization, the output voltage may fluctuate. Please apply the ICs only after careful examination by the customer.
9. The internal power supply VL and gate clamp CLAMP are optimized as a local power supply for the DC/DC control block of the IC. Do not use the VL pin output and the CLAMP pin output.
10. Instructions of pattern layouts
The operation may become unstable due to noise and/or phase lag from the output current when the wire impedance is high, please place the input capacitor(C_{IN}) and the output capacitor (C_L,C_{VL},C_{CLAMP}) as close to the IC as possible.
 - (1) In order to stabilize V_{IN} voltage level, we recommend that a by-pass capacitor (C_{IN}) be connected as close as possible to the V_{IN} and GND pins.
 - (2) Please mount each external component as close to the IC as possible.
 - (3) Wire external components as close to the IC as possible and use thick, short connecting traces to reduce the circuit impedance.
 - (4) Make sure that the GND traces are as thick as possible, as variations in ground potential caused by high ground currents at the time of switching may result in instability of the IC.

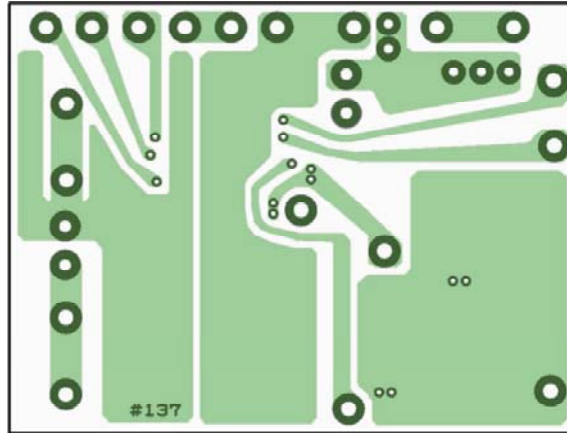
NOTE ON USE (Continued)

10. Instructions of pattern layouts (Continued)

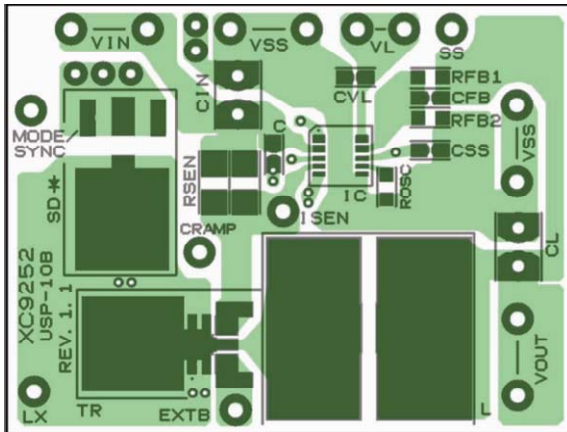
<Reference Pattern Layout>



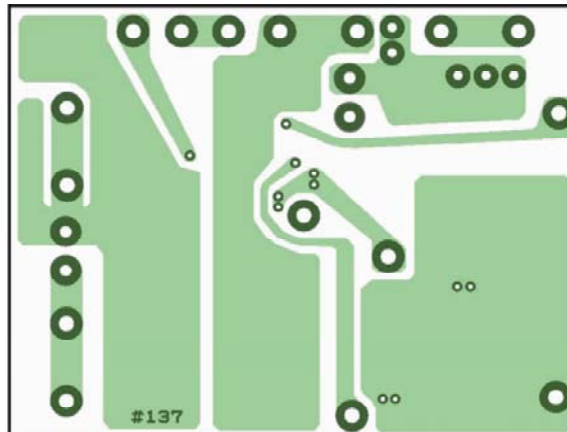
TSSOP-16 (Front)



TSSOP-16 (Back)



USP-10B (Front)



USP-10B (Back)

11. In general, semiconductor components have a possibility to have variation of electrical specifications due to the (cosmic) radiation exposure. Therefore this product has the same possibility. Please inform us in advance if your system might have a possibility to be exposed to the (cosmic) radiation in the production process (assembly, test, etc.).

12. Torex places an importance on improving our products and their reliability.

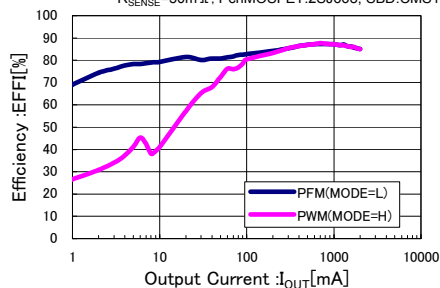
We request that users incorporate fail-safe designs and post-aging protection treatment when using Torex products in their systems.

■ TYPICAL PERFORMANCE CHARACTERISTICS

(1) Efficiency vs. Output current

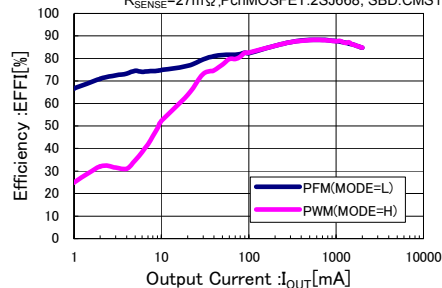
XC9252x08A($V_{IN}=12V$, $V_{OUT}=3.3V$, $f_{OSC}=280kHz$)

$L=22\mu H$ (CLF12555-220M), $C_{IN}=10\mu F$ (GRM32ER71H106KA12L),
 $R_{OSC}=300k\Omega$, $C_L=22\mu F \times 2$ (GRM32ER71E226KE15L),
 $R_{SENSE}=50m\Omega$, PchMOSFET:2SJ668, SBD:CMS15



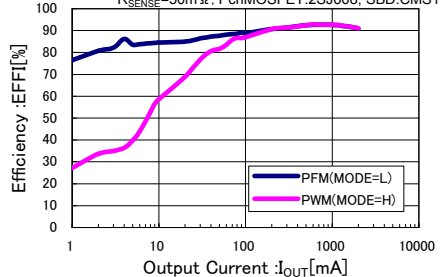
XC9252x08A($V_{IN}=12V$, $V_{OUT}=3.3V$, $f_{OSC}=460kHz$)

$L=10\mu H$ (CLF10040-100M), $C_{IN}=10\mu F$ (GRM32ER71H106KA12L),
 $R_{OSC}=160k\Omega$, $C_L=22\mu F$ (GRM32ER71E226KE15L),
 $R_{SENSE}=27m\Omega$, PchMOSFET:2SJ668, SBD:CMS15



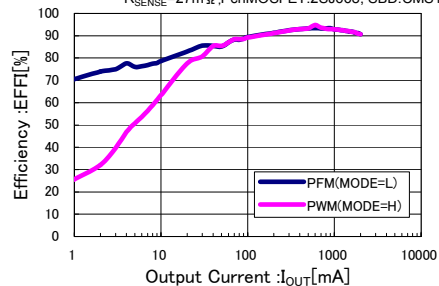
XC9252x08A($V_{IN}=12V$, $V_{OUT}=5.7V$, $f_{OSC}=280kHz$)

$L=22\mu H$ (CLF12555-220M), $C_{IN}=10\mu F$ (GRM32ER71H106KA12L),
 $R_{OSC}=300k\Omega$, $C_L=22\mu F \times 2$ (GRM32ER71E226KE15L),
 $R_{SENSE}=50m\Omega$, PchMOSFET:2SJ668, SBD:CMS15



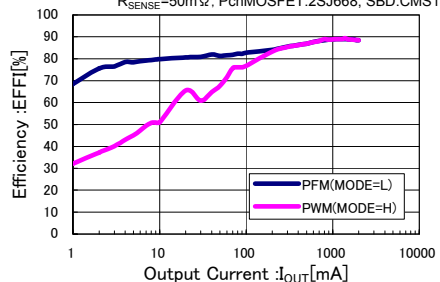
XC9252x08A($V_{IN}=12V$, $V_{OUT}=5.7V$, $f_{OSC}=460kHz$)

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 $R_{SENSE}=27m\Omega$, PchMOSFET:2SJ668, SBD:CMS15



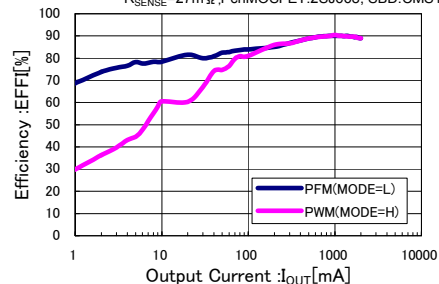
XC9252x08A($V_{IN}=24V$, $V_{OUT}=5.7V$, $f_{OSC}=280kHz$)

$L=22\mu H$ (CLF12555-220M), $C_{IN}=10\mu F$ (GRM32ER71H106KA12L),
 $R_{OSC}=300k\Omega$, $C_L=22\mu F \times 2$ (GRM32ER71E226KE15L),
 $R_{SENSE}=50m\Omega$, PchMOSFET:2SJ668, SBD:CMS15



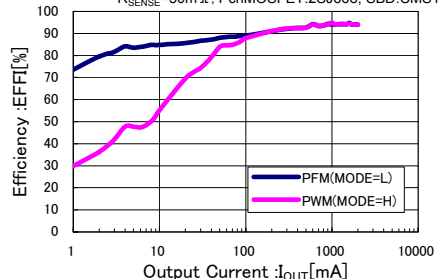
XC9252x08A($V_{IN}=24V$, $V_{OUT}=5.7V$, $f_{OSC}=460kHz$)

$L=10\mu H$ (CLF10040-100M), $C_{IN}=10\mu F$ (GRM32ER71H106KA12L),
 $R_{OSC}=160k\Omega$, $C_L=22\mu F$ (GRM32ER71E226KE15L),
 $R_{SENSE}=27m\Omega$, PchMOSFET:2SJ668, SBD:CMS15



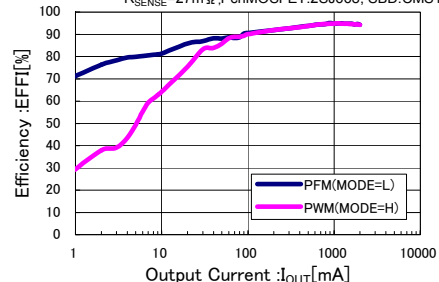
XC9252x08A($V_{IN}=24V$, $V_{OUT}=12V$, $f_{OSC}=280kHz$)

$L=22\mu H$ (CLF12555-220M), $C_{IN}=10\mu F$ (GRM32ER71H106KA12L),
 $R_{OSC}=300k\Omega$, $C_L=22\mu F \times 2$ (GRM32ER71E226KE15L),
 $R_{SENSE}=50m\Omega$, PchMOSFET:2SJ668, SBD:CMS15



XC9252x08A($V_{IN}=24V$, $V_{OUT}=12V$, $f_{OSC}=460kHz$)

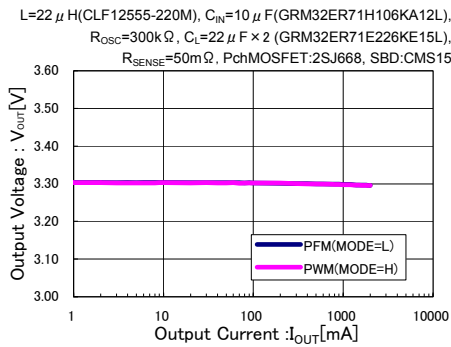
$L=10\mu H$ (CLF10040-100M), $C_{IN}=10\mu F$ (GRM32ER71H106KA12L),
 $R_{OSC}=160k\Omega$, $C_L=22\mu F$ (GRM32ER71E226KE15L),
 $R_{SENSE}=27m\Omega$, PchMOSFET:2SJ668, SBD:CMS15



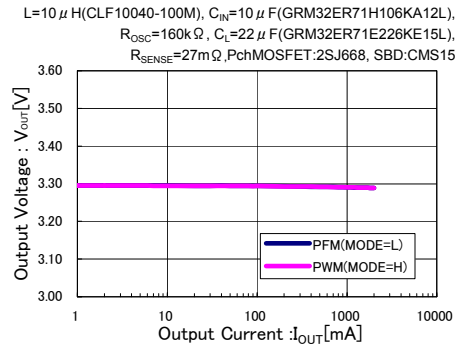
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(2) Output Voltage vs. Output Current

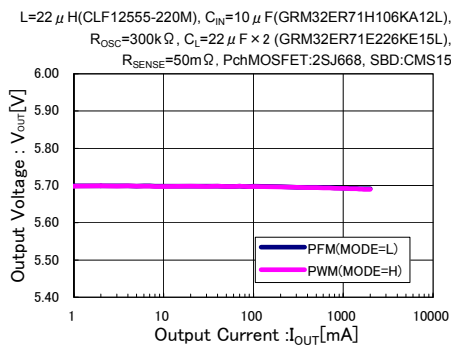
XC9252x08A($V_{IN}=12V$, $V_{OUT}=3.3V$, $f_{OSC}=280kHz$)



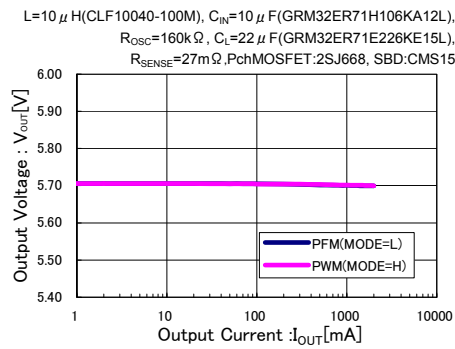
XC9252x08A($V_{IN}=12V$, $V_{OUT}=3.3V$, $f_{OSC}=460kHz$)



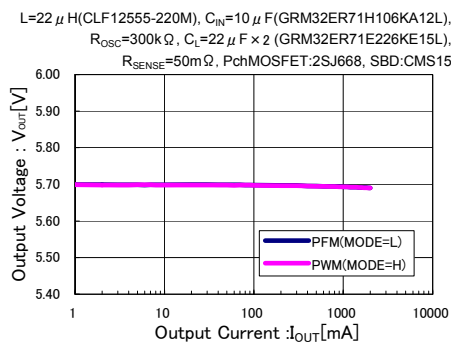
XC9252x08A($V_{IN}=12V$, $V_{OUT}=5.7V$, $f_{OSC}=280kHz$)



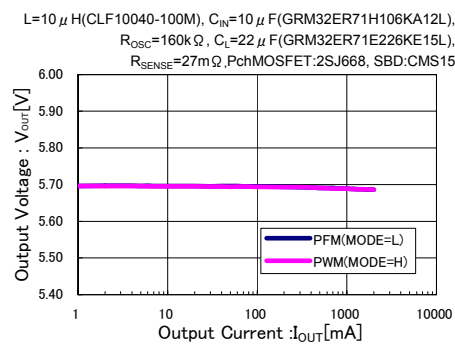
XC9252x08A($V_{IN}=12V$, $V_{OUT}=5.7V$, $f_{OSC}=460kHz$)



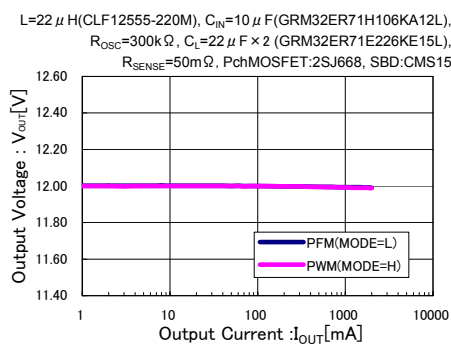
XC9252x08A($V_{IN}=24V$, $V_{OUT}=5.7V$, $f_{OSC}=280kHz$)



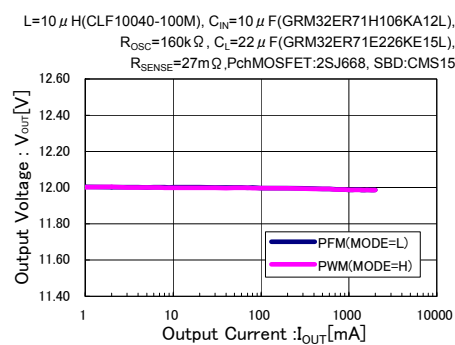
XC9252x08A($V_{IN}=24V$, $V_{OUT}=5.7V$, $f_{OSC}=460kHz$)



XC9252x08A($V_{IN}=24V$, $V_{OUT}=12V$, $f_{OSC}=280kHz$)

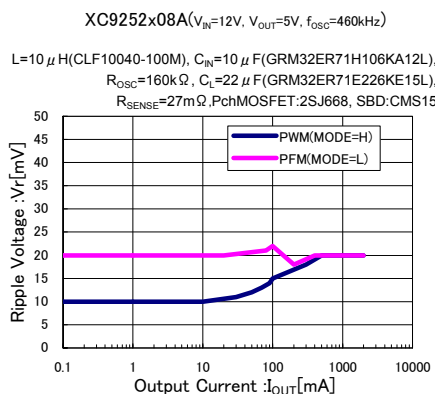
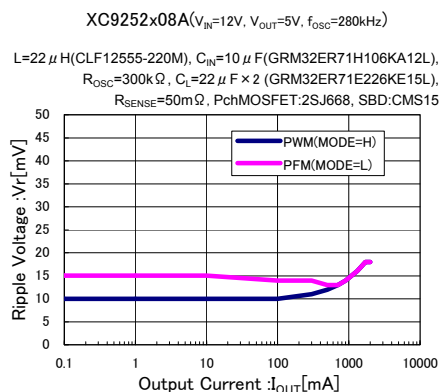


XC9252x08A($V_{IN}=24V$, $V_{OUT}=12V$, $f_{OSC}=460kHz$)



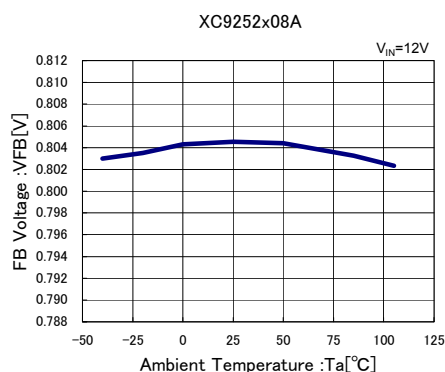
■ TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(3) Ripple Voltage vs. Output Current

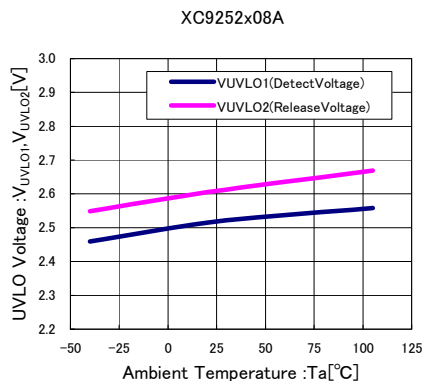


※ when the MODE/SYNC pin is "L", ripple voltage will increase while the PWM and PFM controls switch depending on the conditions of input and output voltage, peripheral components. The ripple voltage can be minimized by operating PWM control state, which the MODE/SYNC pin is "H" or the external clock is synchronized.

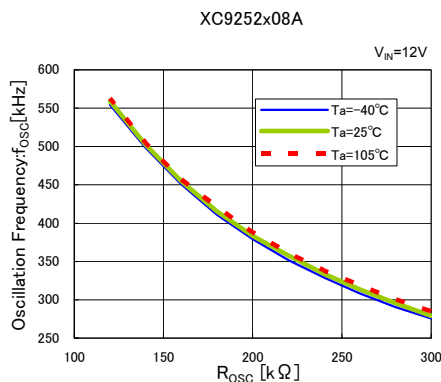
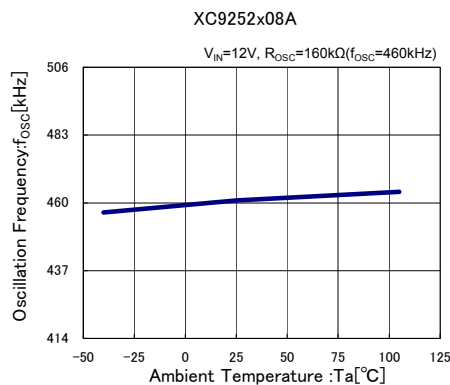
(4) FB Voltage vs. Ambient Temperature



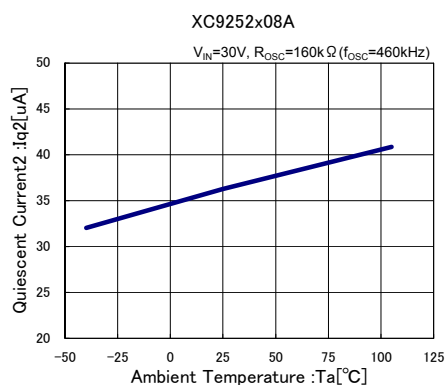
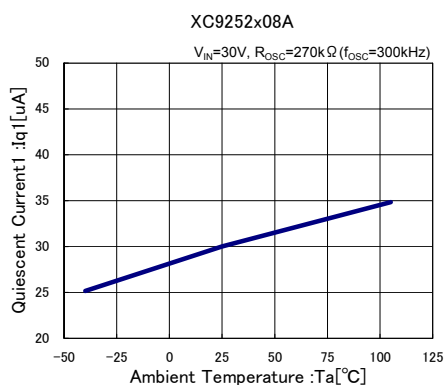
(5) UVLO Voltage vs. Ambient Temperature



(6) Oscillation Frequency vs. Ambient Temperature

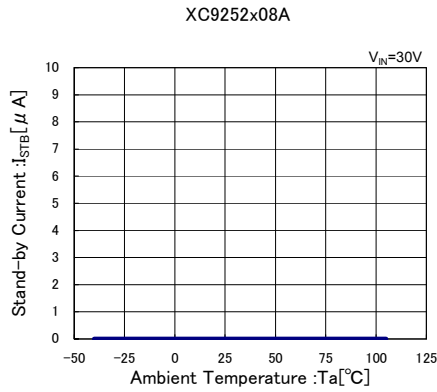


(7) Quiescent Current vs. Ambient Temperature

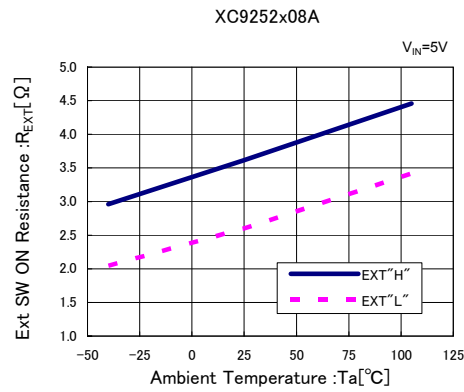


TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

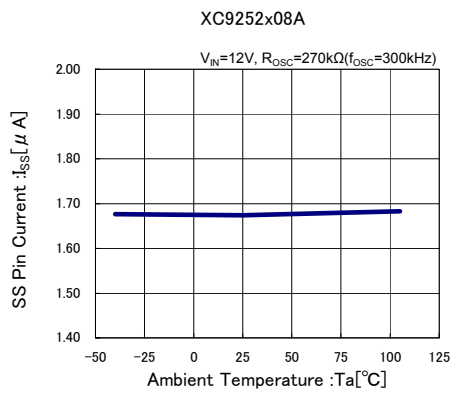
(8) Stand-by Current vs. Ambient Temperature



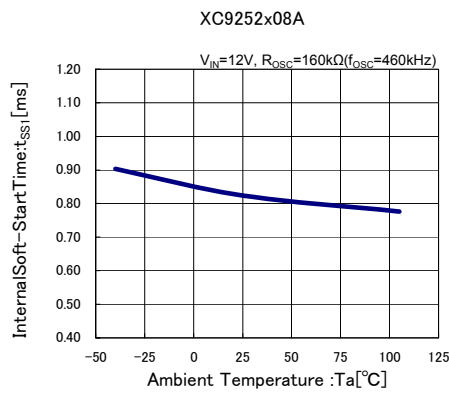
(9) Ext SW ON Resistance vs. Ambient Temperature



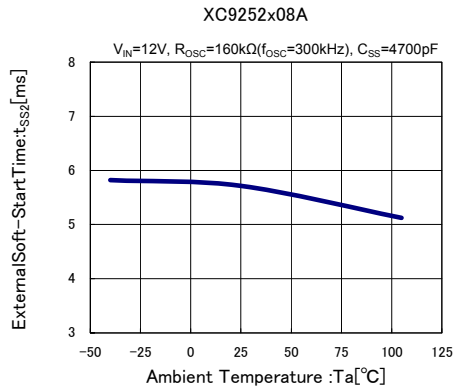
(10) SS Pin Current vs. Ambient Temperature



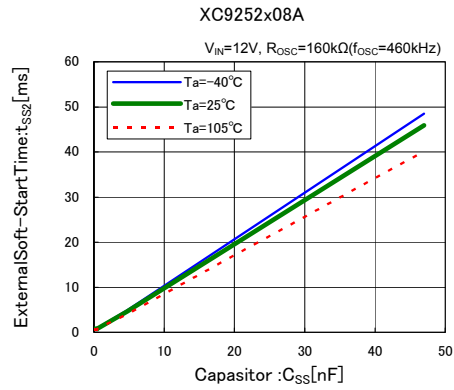
(11) Internal Soft-Start Time vs. Ambient Temperature



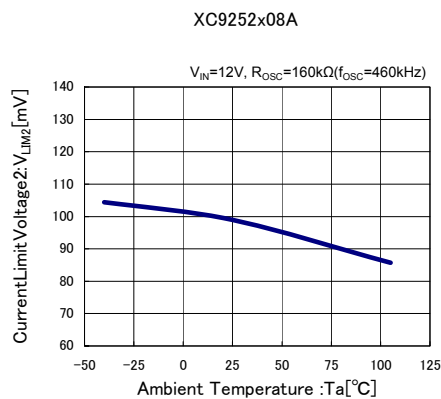
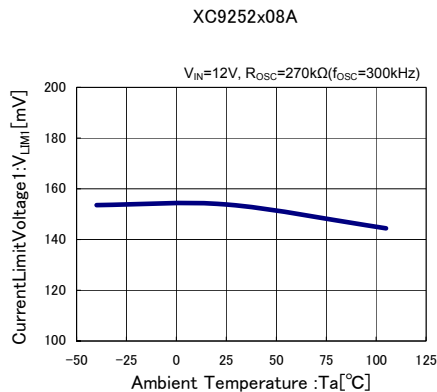
(12) External Soft-Start Time vs. Ambient Temperature



(13) External Soft-Start Time vs. CSS



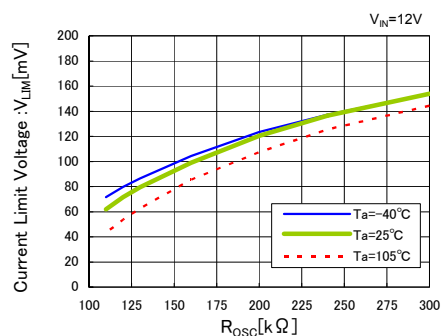
(14) Current Limit Voltage vs. Ambient Temperature



■ TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

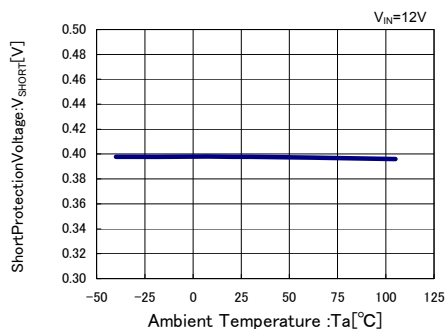
(15) Current Limit Voltage vs. R_{OSC}

XC9252x08A



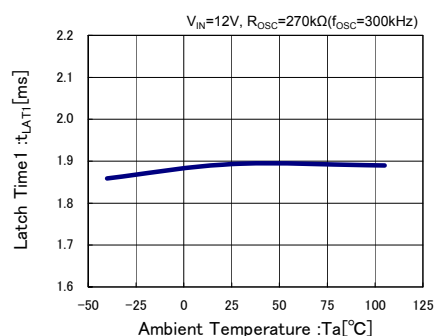
(16) Short Protection Threshold Voltage vs. Temperature

XC9252x08A

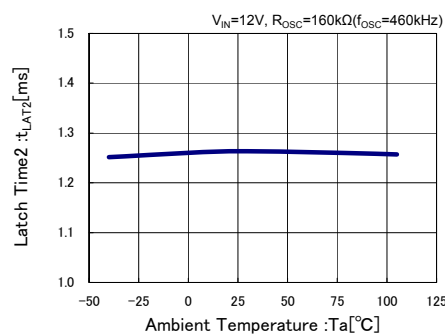


(17) Latch Time vs. Ambient Temperature

XC9252C08A

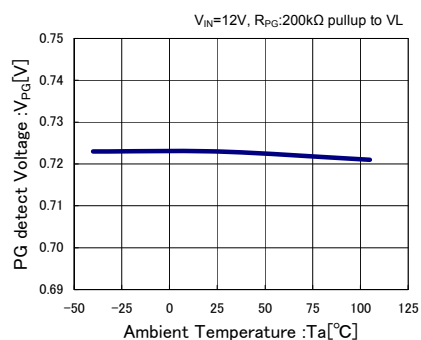


XC9252C08A



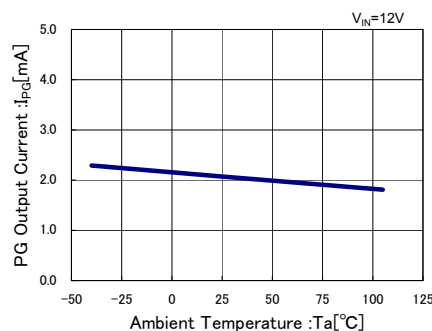
(18) PG Detect Voltage vs. Ambient Temperature

XC9252x08A



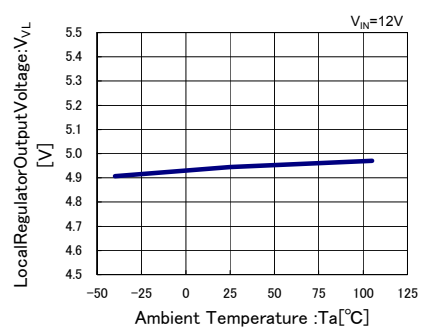
(19) PG Output Current vs. Ambient Temperature

XC9252x08A



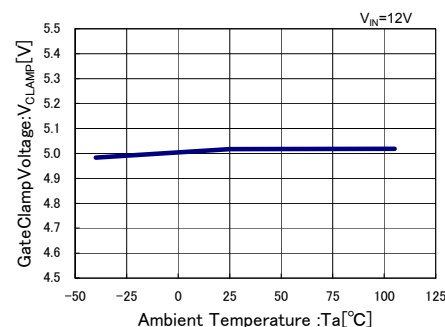
(20) Local Regulator Output Voltage vs. Ambient Temperature

XC9252x08A



(21) Gate Clamp Voltage vs. Ambient Temperature

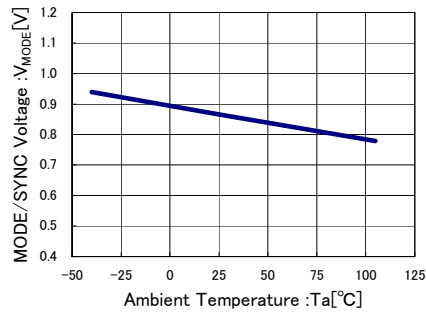
XC9252x08A



TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

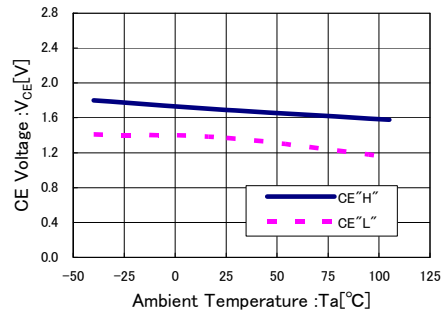
(22) MODE/SYNC Voltage vs. Ambient Temperature

XC9252x08A



(23) CE Voltage vs. Ambient Temperature

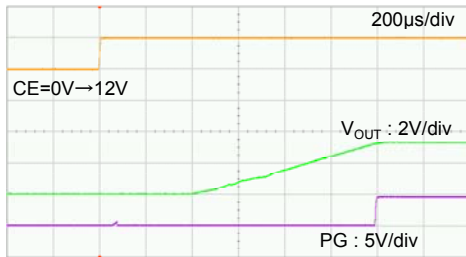
XC9252x08A



(24) CE Rising Response

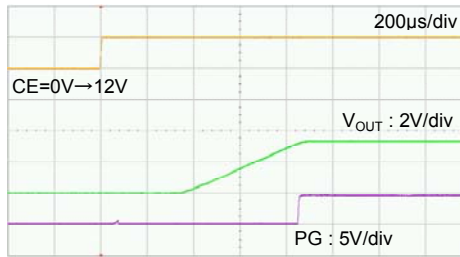
XC9252x08A, $f_{OSC}=300kHz$

$V_{IN}=12V$, $V_{CE}=0 \rightarrow 12V$, $V_{OUT}=3.3V$, $I_{OUT}=1A$, $C_{SS}:OPEN$
 $L=22\mu H$ (CLF12555-220M), $C_{IN}=10\mu F$ (GRM32ER71H106KA12L),
 $R_{OSC}=270k\Omega$, $C_t=22\mu F \times 2$ (GRM32ER71E226KE15L),
 $R_{SENSE}=50m\Omega$, PchMOSFET:2SJ668, SBD:CMS15



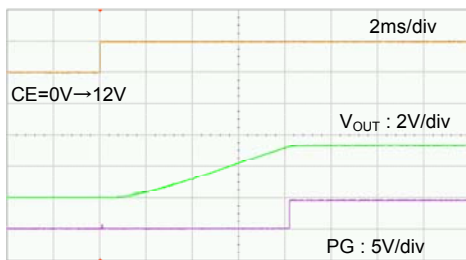
XC9252x08A, $f_{OSC}=460kHz$

$V_{IN}=12V$, $V_{CE}=0 \rightarrow 12V$, $V_{OUT}=3.3V$, $I_{OUT}=1A$, $C_{SS}:OPEN$
 $L=10\mu H$ (CLF10040-100M), $C_{IN}=10\mu F$ (GRM32ER71H106KA12L),
 $R_{OSC}=160k\Omega$, $C_t=22\mu F$ (GRM32ER71E226KE15L),
 $R_{SENSE}=27m\Omega$, PchMOSFET:2SJ668, SBD:CMS15



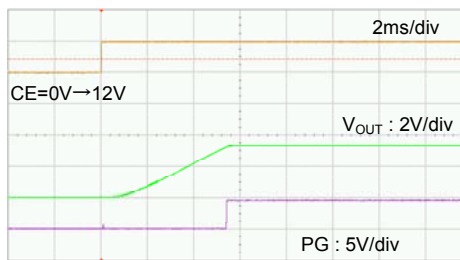
XC9252x08A, $f_{OSC}=300kHz$

$V_{IN}=12V$, $V_{CE}=0 \rightarrow 12V$, $V_{OUT}=3.3V$, $I_{OUT}=1A$, $C_{SS}:4700pF$
 $L=22\mu H$ (CLF12555-220M), $C_{IN}=10\mu F$ (GRM32ER71H106KA12L),
 $R_{OSC}=270k\Omega$, $C_t=22\mu F \times 2$ (GRM32ER71E226KE15L),
 $R_{SENSE}=50m\Omega$, PchMOSFET:2SJ668, SBD:CMS15



XC9252x08A, $f_{OSC}=460kHz$

$V_{IN}=12V$, $V_{CE}=0 \rightarrow 12V$, $V_{OUT}=3.3V$, $I_{OUT}=1A$, $C_{SS}:4700pF$
 $L=10\mu H$ (CLF10040-100M), $C_{IN}=10\mu F$ (GRM32ER71H106KA12L),
 $R_{OSC}=160k\Omega$, $C_t=22\mu F$ (GRM32ER71E226KE15L),
 $R_{SENSE}=27m\Omega$, PchMOSFET:2SJ668, SBD:CMS15

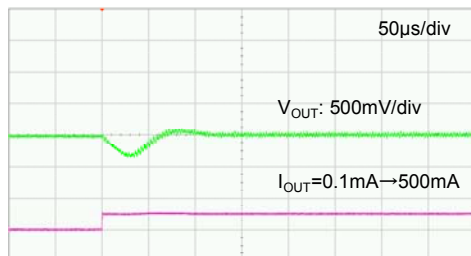


■ TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(25) Load Transient Response (MODE=L, PFM/PWM Control)

XC9252x08A, $f_{OSC}=300kHz$

$V_{IN}=12V$, $V_{OUT}=3.3V$, $I_{OUT}=0.1mA \rightarrow 500mA$
 $L=22\mu H$ (CLF12555-220M), $C_{IN}=10\mu F$ (GRM32ER71H106KA12L),
 $R_{OSC}=270k\Omega$, $C_L=22\mu F \times 2$ (GRM32ER71E226KE15L),
 $R_{SENSE}=50m\Omega$, PchMOSFET:2SJ668, SBD:CMS15



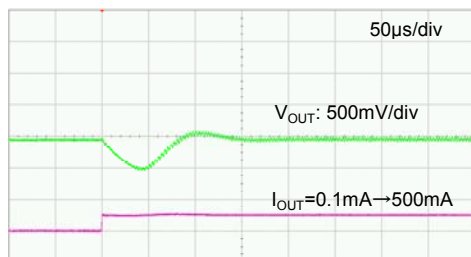
XC9252x08A, $f_{OSC}=300kHz$

$V_{IN}=12V$, $V_{OUT}=3.3V$, $I_{OUT}=500mA \rightarrow 0.1mA$
 $L=22\mu H$ (CLF12555-220M), $C_{IN}=10\mu F$ (GRM32ER71H106KA12L),
 $R_{OSC}=270k\Omega$, $C_L=22\mu F \times 2$ (GRM32ER71E226KE15L),
 $R_{SENSE}=50m\Omega$, PchMOSFET:2SJ668, SBD:CMS15



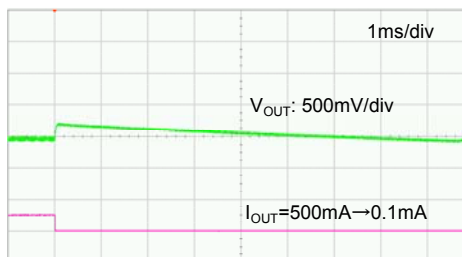
XC9252x08A, $f_{OSC}=300kHz$

$V_{IN}=12V$, $V_{OUT}=5.0V$, $I_{OUT}=0.1mA \rightarrow 500mA$
 $L=22\mu H$ (CLF12555-220M), $C_{IN}=10\mu F$ (GRM32ER71H106KA12L),
 $R_{OSC}=270k\Omega$, $C_L=22\mu F \times 2$ (GRM32ER71E226KE15L),
 $R_{SENSE}=50m\Omega$, PchMOSFET:2SJ668, SBD:CMS15



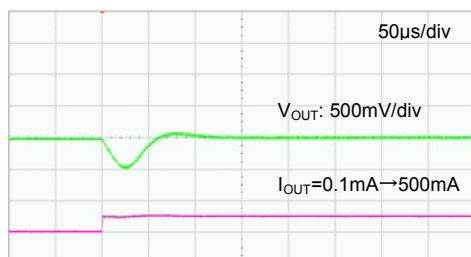
XC9252x08A, $f_{OSC}=300kHz$

$V_{IN}=12V$, $V_{OUT}=5.0V$, $I_{OUT}=500mA \rightarrow 0.1mA$
 $L=22\mu H$ (CLF12555-220M), $C_{IN}=10\mu F$ (GRM32ER71H106KA12L),
 $R_{OSC}=270k\Omega$, $C_L=22\mu F \times 2$ (GRM32ER71E226KE15L),
 $R_{SENSE}=50m\Omega$, PchMOSFET:2SJ668, SBD:CMS15



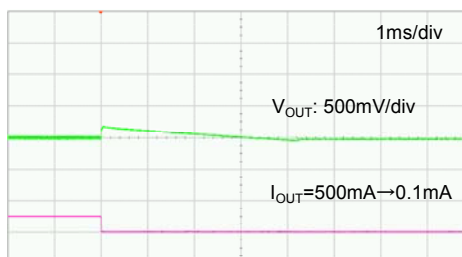
XC9252x08A, $f_{OSC}=460kHz$

$V_{IN}=12V$, $V_{OUT}=3.3V$, $I_{OUT}=0.1mA \rightarrow 500mA$
 $L=10\mu H$ (CLF10040-100M), $C_{IN}=10\mu F$ (GRM32ER71H106KA12L),
 $R_{OSC}=160k\Omega$, $C_L=22\mu F$ (GRM32ER71E226KE15L),
 $R_{SENSE}=27m\Omega$, PchMOSFET:2SJ668, SBD:CMS15



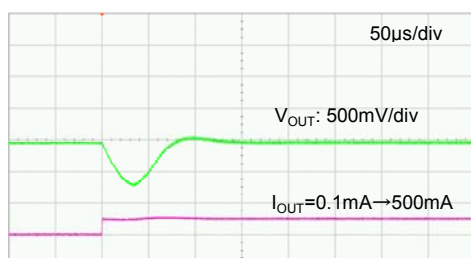
XC9252x08A, $f_{OSC}=460kHz$

$V_{IN}=12V$, $V_{OUT}=3.3V$, $I_{OUT}=500mA \rightarrow 0.1mA$
 $L=10\mu H$ (CLF10040-100M), $C_{IN}=10\mu F$ (GRM32ER71H106KA12L),
 $R_{OSC}=160k\Omega$, $C_L=22\mu F$ (GRM32ER71E226KE15L),
 $R_{SENSE}=27m\Omega$, PchMOSFET:2SJ668, SBD:CMS15



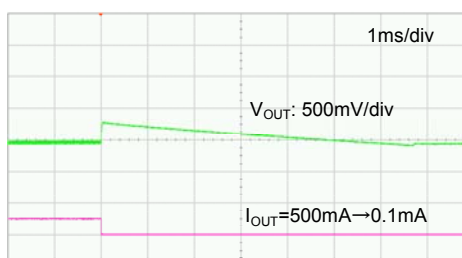
XC9252x08A, $f_{OSC}=460kHz$

$V_{IN}=12V$, $V_{OUT}=5.0V$, $I_{OUT}=0.1mA \rightarrow 500mA$
 $L=10\mu H$ (CLF10040-100M), $C_{IN}=10\mu F$ (GRM32ER71H106KA12L),
 $R_{OSC}=160k\Omega$, $C_L=22\mu F$ (GRM32ER71E226KE15L),
 $R_{SENSE}=27m\Omega$, PchMOSFET:2SJ668, SBD:CMS15



XC9252x08A, $f_{OSC}=460kHz$

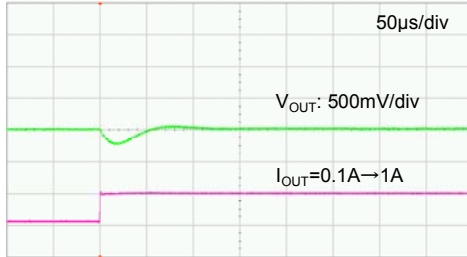
$V_{IN}=12V$, $V_{OUT}=5.0V$, $I_{OUT}=500mA \rightarrow 0.1mA$
 $L=10\mu H$ (CLF10040-100M), $C_{IN}=10\mu F$ (GRM32ER71H106KA12L),
 $R_{OSC}=160k\Omega$, $C_L=22\mu F$ (GRM32ER71E226KE15L),
 $R_{SENSE}=27m\Omega$, PchMOSFET:2SJ668, SBD:CMS15



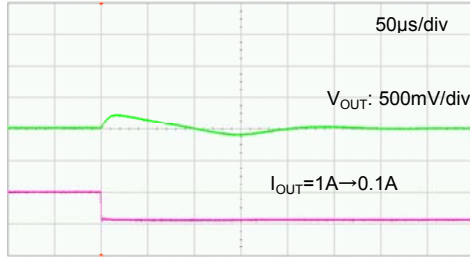
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(26) Load Transient Response (MODE=H, PWM Control)

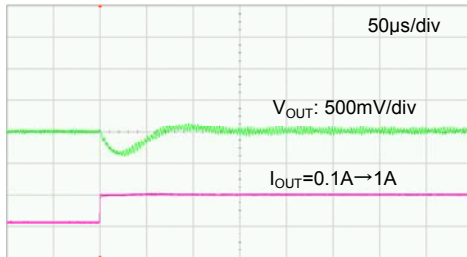
XC9252x08A, $f_{OSC}=300kHz$
 $V_{IN}=12V$, $V_{OUT}=3.3V$, $I_{OUT}=0.1A \rightarrow 1A$
 $L=22\mu H$ (CLF12555-220M), $C_{IN}=10\mu F$ (GRM32ER71H106KA12L),
 $R_{OSC}=270k\Omega$, $C_L=22\mu F \times 2$ (GRM32ER71E226KE15L),
 $R_{SENSE}=50m\Omega$, PchMOSFET:2SJ668, SBD:CMS15



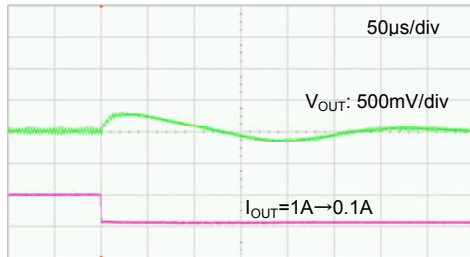
XC9252x08A, $f_{OSC}=300kHz$
 $V_{IN}=12V$, $V_{OUT}=3.3V$, $I_{OUT}=1A \rightarrow 0.1A$
 $L=22\mu H$ (CLF12555-220M), $C_{IN}=10\mu F$ (GRM32ER71H106KA12L),
 $R_{OSC}=270k\Omega$, $C_L=22\mu F \times 2$ (GRM32ER71E226KE15L),
 $R_{SENSE}=50m\Omega$, PchMOSFET:2SJ668, SBD:CMS15



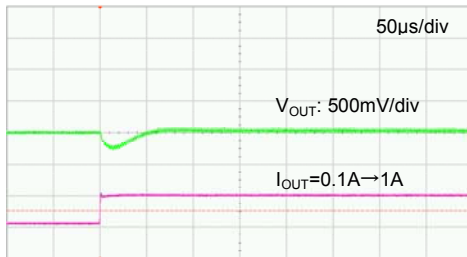
XC9252x08A, $f_{OSC}=300kHz$
 $V_{IN}=12V$, $V_{OUT}=5.0V$, $I_{OUT}=0.1A \rightarrow 1A$
 $L=22\mu H$ (CLF12555-220M), $C_{IN}=10\mu F$ (GRM32ER71H106KA12L),
 $R_{OSC}=270k\Omega$, $C_L=22\mu F \times 2$ (GRM32ER71E226KE15L),
 $R_{SENSE}=50m\Omega$, PchMOSFET:2SJ668, SBD:CMS15



XC9252x08A, $f_{OSC}=300kHz$
 $V_{IN}=12V$, $V_{OUT}=5.0V$, $I_{OUT}=1A \rightarrow 0.1A$
 $L=22\mu H$ (CLF12555-220M), $C_{IN}=10\mu F$ (GRM32ER71H106KA12L),
 $R_{OSC}=270k\Omega$, $C_L=22\mu F \times 2$ (GRM32ER71E226KE15L),
 $R_{SENSE}=50m\Omega$, PchMOSFET:2SJ668, SBD:CMS15



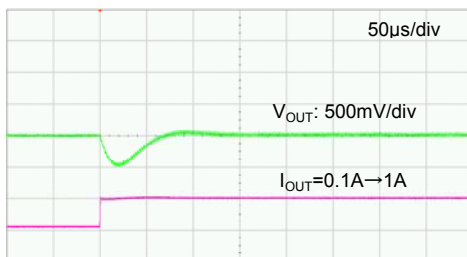
XC9252x08A, $f_{OSC}=460kHz$
 $V_{IN}=12V$, $V_{OUT}=3.3V$, $I_{OUT}=0.1A \rightarrow 1A$
 $L=10\mu H$ (CLF10040-100M), $C_{IN}=10\mu F$ (GRM32ER71H106KA12L),
 $R_{OSC}=160k\Omega$, $C_L=22\mu F$ (GRM32ER71E226KE15L),
 $R_{SENSE}=27m\Omega$, PchMOSFET:2SJ668, SBD:CMS15



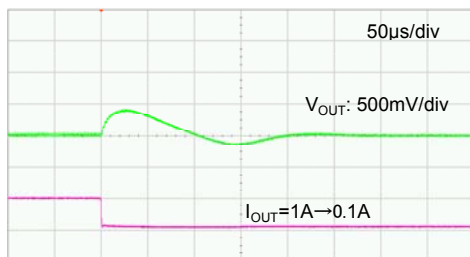
XC9252x08A, $f_{OSC}=460kHz$
 $V_{IN}=12V$, $V_{OUT}=3.3V$, $I_{OUT}=1A \rightarrow 0.1A$
 $L=10\mu H$ (CLF10040-100M), $C_{IN}=10\mu F$ (GRM32ER71H106KA12L),
 $R_{OSC}=160k\Omega$, $C_L=22\mu F$ (GRM32ER71E226KE15L),
 $R_{SENSE}=27m\Omega$, PchMOSFET:2SJ668, SBD:CMS15



XC9252x08A, $f_{OSC}=460kHz$
 $V_{IN}=12V$, $V_{OUT}=5.0V$, $I_{OUT}=0.1A \rightarrow 1A$
 $L=10\mu H$ (CLF10040-100M), $C_{IN}=10\mu F$ (GRM32ER71H106KA12L),
 $R_{OSC}=160k\Omega$, $C_L=22\mu F$ (GRM32ER71E226KE15L),
 $R_{SENSE}=27m\Omega$, PchMOSFET:2SJ668, SBD:CMS15



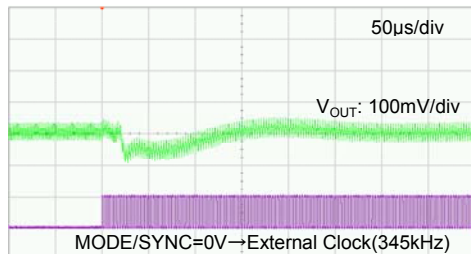
XC9252x08A, $f_{OSC}=460kHz$
 $V_{IN}=12V$, $V_{OUT}=5.0V$, $I_{OUT}=1A \rightarrow 0.1A$
 $L=10\mu H$ (CLF10040-100M), $C_{IN}=10\mu F$ (GRM32ER71H106KA12L),
 $R_{OSC}=160k\Omega$, $C_L=22\mu F$ (GRM32ER71E226KE15L),
 $R_{SENSE}=27m\Omega$, PchMOSFET:2SJ668, SBD:CMS15



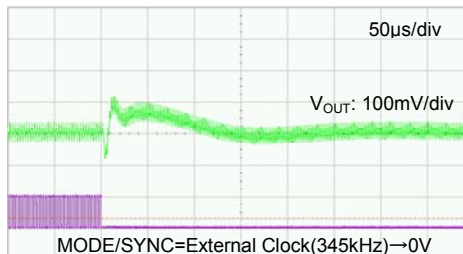
■ TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(27) Transient Response (MODE/SYNC=L ⇄ External Clock) (Continued)

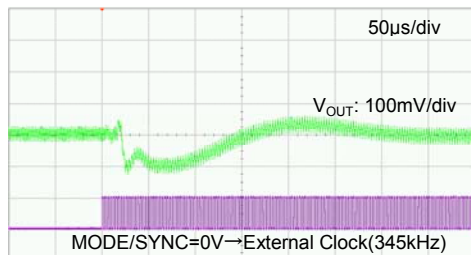
XC9252x08A, $f_{OSC}=460kHz$
 $V_{IN}=12V$, $V_{OUT}=3.3V$, $I_{OUT}=1A$, $f_{OSC}=460kHz \rightarrow 345kHz$
 $L=10\mu H$ (CLF10040-100M), $C_{IN}=10\mu F$ (GRM32ER71H106KA12L),
 $R_{OSC}=160k\Omega$, $C_L=22\mu F$ (GRM32ER71E226KE15L),
 $R_{SENSE}=27m\Omega$, PchMOSFET:2SJ668, SBD:CMS15



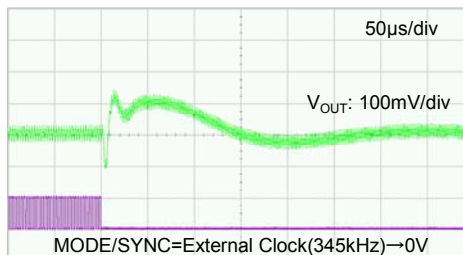
XC9252x08A, $f_{OSC}=460kHz$
 $V_{IN}=12V$, $V_{OUT}=3.3V$, $I_{OUT}=1A$, $f_{OSC}=345kHz \rightarrow 460kHz$
 $L=10\mu H$ (CLF10040-100M), $C_{IN}=10\mu F$ (GRM32ER71H106KA12L),
 $R_{OSC}=160k\Omega$, $C_L=22\mu F$ (GRM32ER71E226KE15L),
 $R_{SENSE}=27m\Omega$, PchMOSFET:2SJ668, SBD:CMS15



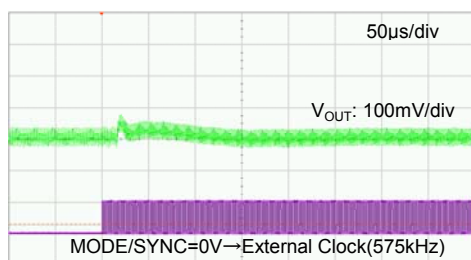
XC9252x08A, $f_{OSC}=460kHz$
 $V_{IN}=12V$, $V_{OUT}=5.0V$, $I_{OUT}=1A$, $f_{OSC}=460kHz \rightarrow 345kHz$
 $L=10\mu H$ (CLF10040-100M), $C_{IN}=10\mu F$ (GRM32ER71H106KA12L),
 $R_{OSC}=160k\Omega$, $C_L=22\mu F$ (GRM32ER71E226KE15L),
 $R_{SENSE}=27m\Omega$, PchMOSFET:2SJ668, SBD:CMS15



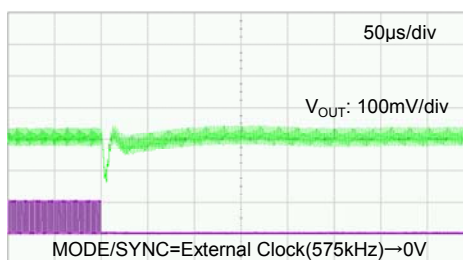
XC9252x08A, $f_{OSC}=460kHz$
 $V_{IN}=12V$, $V_{OUT}=5.0V$, $I_{OUT}=1A$, $f_{OSC}=345kHz \rightarrow 460kHz$
 $L=10\mu H$ (CLF10040-100M), $C_{IN}=10\mu F$ (GRM32ER71H106KA12L),
 $R_{OSC}=160k\Omega$, $C_L=22\mu F$ (GRM32ER71E226KE15L),
 $R_{SENSE}=27m\Omega$, PchMOSFET:2SJ668, SBD:CMS15



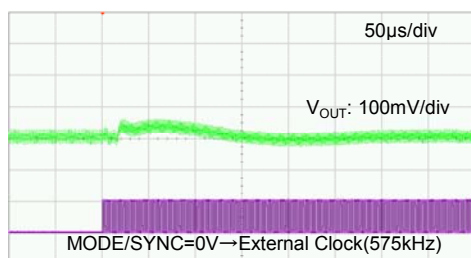
XC9252x08A, $f_{OSC}=460kHz$
 $V_{IN}=12V$, $V_{OUT}=3.3V$, $I_{OUT}=1A$, $f_{OSC}=460kHz \rightarrow 575kHz$
 $L=10\mu H$ (CLF10040-100M), $C_{IN}=10\mu F$ (GRM32ER71H106KA12L),
 $R_{OSC}=160k\Omega$, $C_L=22\mu F$ (GRM32ER71E226KE15L),
 $R_{SENSE}=27m\Omega$, PchMOSFET:2SJ668, SBD:CMS15



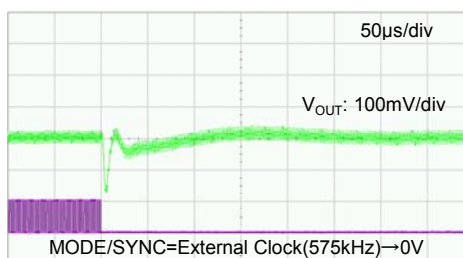
XC9252x08A, $f_{OSC}=460kHz$
 $V_{IN}=12V$, $V_{OUT}=3.3V$, $I_{OUT}=1A$, $f_{OSC}=575kHz \rightarrow 460kHz$
 $L=10\mu H$ (CLF10040-100M), $C_{IN}=10\mu F$ (GRM32ER71H106KA12L),
 $R_{OSC}=160k\Omega$, $C_L=22\mu F$ (GRM32ER71E226KE15L),
 $R_{SENSE}=27m\Omega$, PchMOSFET:2SJ668, SBD:CMS15



XC9252x08A, $f_{OSC}=460kHz$
 $V_{IN}=12V$, $V_{OUT}=5.0V$, $I_{OUT}=1A$, $f_{OSC}=460kHz \rightarrow 575kHz$
 $L=10\mu H$ (CLF10040-100M), $C_{IN}=10\mu F$ (GRM32ER71H106KA12L),
 $R_{OSC}=160k\Omega$, $C_L=22\mu F$ (GRM32ER71E226KE15L),
 $R_{SENSE}=27m\Omega$, PchMOSFET:2SJ668, SBD:CMS15

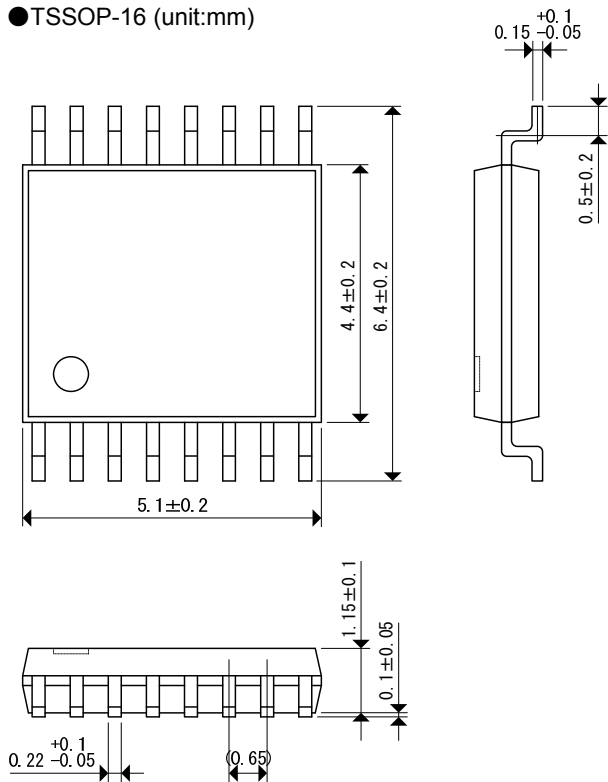


XC9252x08A, $f_{OSC}=460kHz$
 $V_{IN}=12V$, $V_{OUT}=5.0V$, $I_{OUT}=1A$, $f_{OSC}=575kHz \rightarrow 460kHz$
 $L=10\mu H$ (CLF10040-100M), $C_{IN}=10\mu F$ (GRM32ER71H106KA12L),
 $R_{OSC}=160k\Omega$, $C_L=22\mu F$ (GRM32ER71E226KE15L),
 $R_{SENSE}=27m\Omega$, PchMOSFET:2SJ668, SBD:CMS15

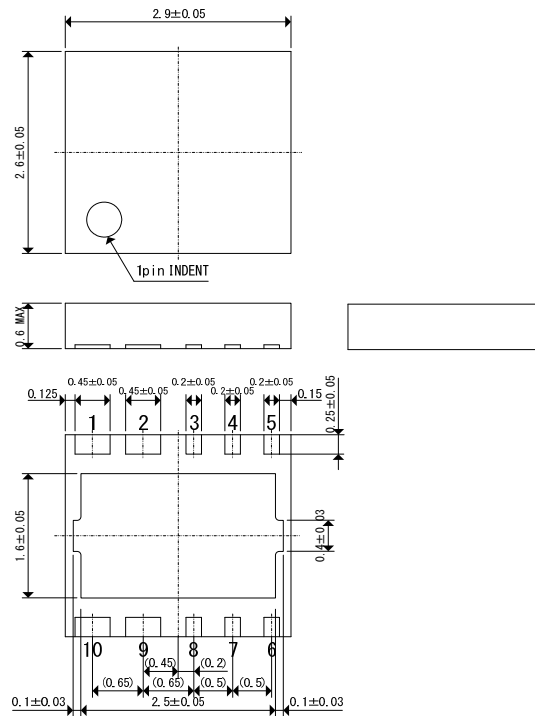


PACKAGING INFORMATION

●TSSOP-16 (unit:mm)



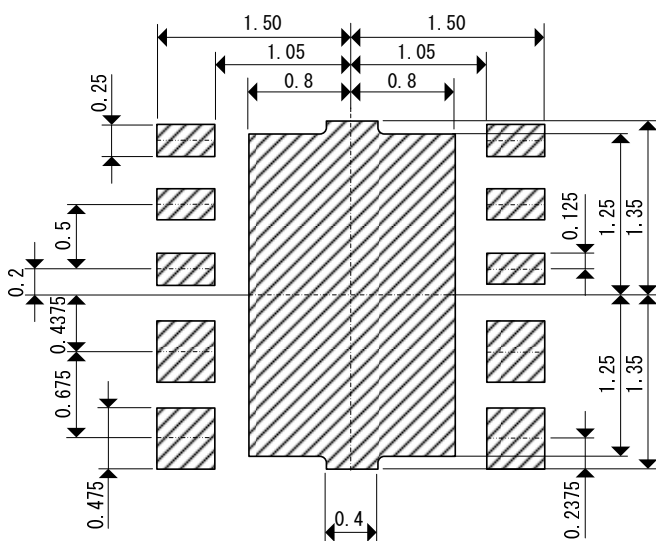
●USP-10B (unit: mm)



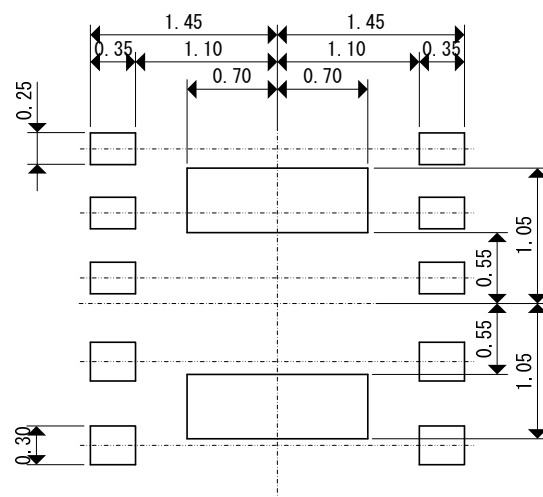
* The side of pins are not gilded, but nickel is used.

* Pin #1, #2, #9 and #10 is wider than other pins.

●USP-10B (unit: mm) Reference Pattern Layout

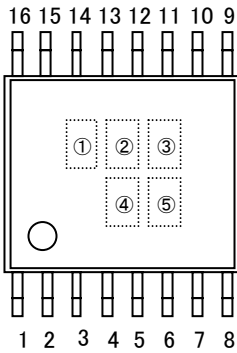


●USP-10B (unit: mm) Reference Metal Mask Design

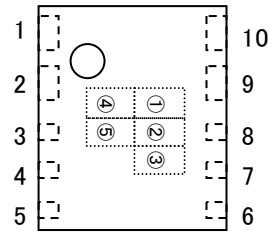


■ MARKING RULE

TSSOP-16



USP-10B



① represents products series

MARK	PRODUCT SERIES
1	XC9252*****-G

② represents products type

MARK	TYPE	PRODUCT SERIES
A	Standard type	XC9252A*****-G
B	Without chip enable, power-good	XC9252B*****-G
C	Standard type with latch protection	XC9252C*****-G

③ represents reference voltage and oscillation frequency

MARK	VOLTAGE (V)	OSCILLATION FREQUENCY	PRODUCT SERIES
A	0.8	Adjustable	XC9252*08A**-G

④⑤ represents production lot number

01~09, 0A~0Z, 11~9Z, A1~A9, AA~AZ, B1~ZZ in order.

(G, I, J, O, Q, W excluded)

* No character inversion used.

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